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# LNW80

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TREATY # 1

DELETE { C41 FROM SHEET 6 SHOULD BE: NOT USED  
ON SHEET 13 CHANGE 6.8 mfd Qty to 16, delete 41

## ERRATA #2

The schematic diagram, labeled 'FIG. 1', illustrates the internal circuitry of a television receiver. It is divided into several functional sections:

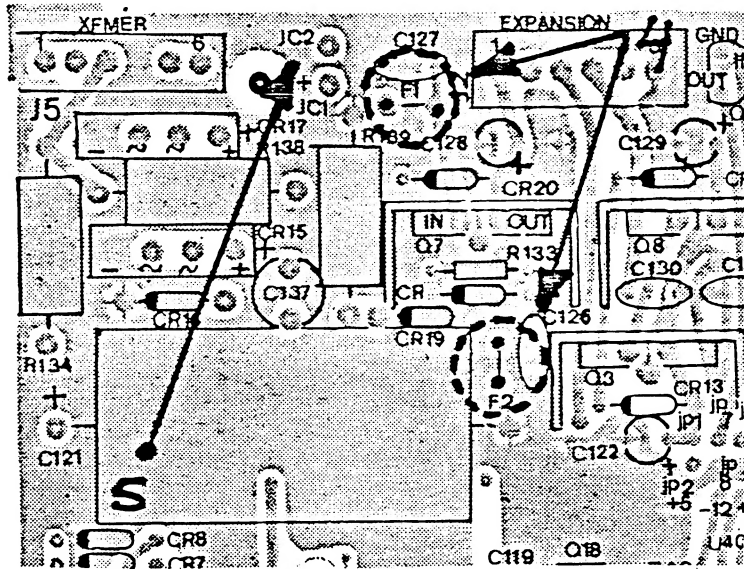
- Power Supply Section:** Features a 2.0A power transformer (T1) connected to a 120V AC source. The secondary winding provides 120V, 0V, and 120V. The circuit includes a 2.0A fuse (F2), a 2200µF capacitor (C1), and a 35VDC regulator (U1). A 74123 timer (U2) is used for timing purposes.
- Video Section:** Includes a 74124 timer (U3) and a 74125 timer (U4). The circuit is connected to a 120V AC source and a 120V DC source. It includes a 2.0A fuse (F2) and a 2200µF capacitor (C1).
- Audio Section:** Features a 74123 timer (U2) and a 74124 timer (U3). The circuit is connected to a 120V AC source and a 120V DC source. It includes a 2.0A fuse (F2) and a 2200µF capacitor (C1).
- Control Section:** Includes a 74123 timer (U2) and a 74124 timer (U3). The circuit is connected to a 120V AC source and a 120V DC source. It includes a 2.0A fuse (F2) and a 2200µF capacitor (C1).

The schematic is annotated with component values and pin numbers. A list of component values is provided at the bottom right:

U1, 15, 16, 17, 20, 28, 29, 30, 31	U6, 83
32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51	103
52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82	120
83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200	130

## ERRATA # 3 (CONT)

4. INSTALL 4.0 A FAST BLOW FUSE AT F1 AND 2.0 AMP FAST BLOW FUSE AT F2. THIS CAN BE DONE WITH INLINE FUSE HOLDERS WIRED AT F1 & F2 OR F1 and F2 CAN BE PIGTAIL FUSES INSTALLED STANDING VERTICAL WITH ONE LEAD EXTENDED TO REACH. BE SURE TO COVER FUSE WITH INSULATION



TO PROTECT AGAINST SHORTING TO HEATSINKS AND CONNECTORS. F1 AND F2 CAN ALSO BE INSTALLED IN CHASSIS MOUNTED FUSE HOLDERS WIRED TO F1 AND F2.

5. WIRE C141 (15,000  $\mu$ d 16V) electrolytic CAPACITOR TO JC1 and JC2  
WIRE THE POSITIVE (+) END OF C141 TO JC1  
AND THE NEGATIVE (-) END OF C141 TO JC2  
C141 MUST BE CHASSIS MOUNTED.

## ERRATA # 4

## KEYBOARD WIRING NOTICE

### SPECIAL NOTICE

WHEN WIRING A KEYBOARD TO CONNECTOR J4 MAKE SURE IT WIRES POINT TO POINT. WHEN

INSTALLING THE LNW KEYBOARD MAKE SURE:

1. USE HEADERS (MAKE 40 COND.) ON THE PC BOARDS.  
DO NOT USE FEMALE SOCKET TYPES!

2. USE A CABLE WITH FEMALE SOCKET CONNECTORS AT EACH END.

HERE ARE THE PART NUMBERS WE RECOMMEND:

(1 REQUIRED) HEADERS - AP PRODUCTS # 923865-R

(1 REQUIRED) CABLE AP PRODUCTS # 924005-18R

WE HAVE BOTH OF THE ABOVE IN OUR KEYBOARD CABLE KIT, KIT80-4

# ERRATA # 3

## ASSEMBLY ERRATA

USE THE FOLLOWING INSTRUCTIONS TO  
REPLACE THE SPECIAL WIRING SECTION  
OF SECTION 4.2 ON PAGE 16

### 4.2 SPECIFIC ASSEMBLY INSTRUCTIONS

#### SPECIAL WIRING

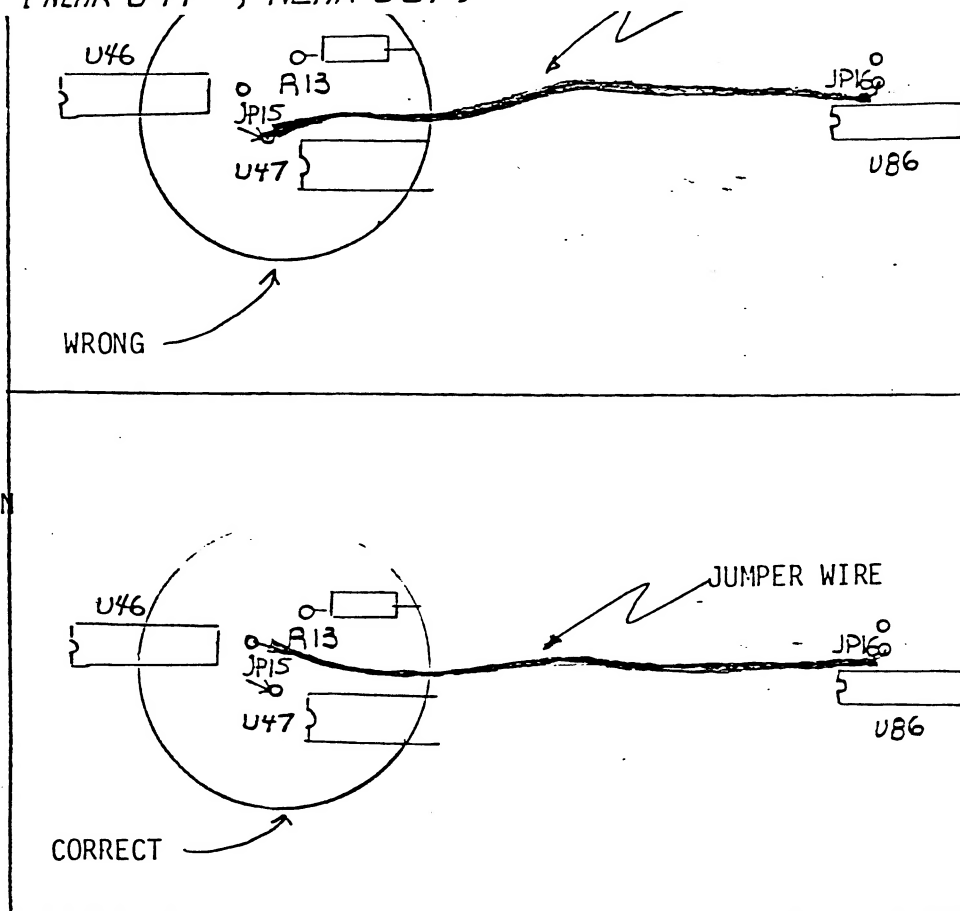
The following three special assembly instructions should be accurately incorporated:

1. Add a jumper wire (insulated wire) from:  
JP15 to JP16  
(NEAR U47 ; NEAR U87)

#### NOTE:

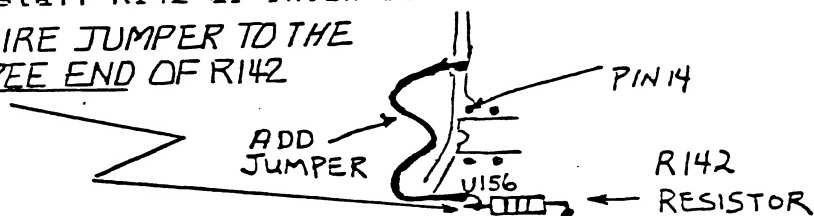
THERE IS AN  
ERROR IN THE SILK  
SCREENED REFERENCE  
FOR jp15. INSTALL  
THE JUMPER WIRE  
TO THE PAD AT THE  
TOP OF THE 'j' IN  
THE jp15 SILK  
SCREEN REFERENCE

NOTE THE CORRECT  
JUMPER INSTALLATION  
TO THE RIGHT



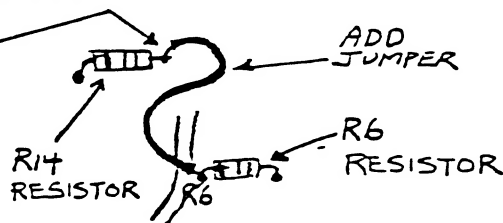
2. Install R142 as shown below:

WIRE JUMPER TO THE  
FREE END OF R142



3. Install R14 as shown below:

WIRE JUMPER TO THE  
FREE END OF R14



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## 1.0 INTRODUCTION

LNW Research Corporation thanks you for selecting the LNW80 as your personal or business computer. We at LNW Research have strived to produce the highest quality products based on state of the art technology and we feel that the LNW80 exemplifies this goal.

### PRELIMINARY MANUAL

This is a PRELIMINARY LNW80 MANUAL. Any additions to this manual will be sent to you at no charge if you would return the enclosed mailing label with your name and address.

FROM	NAME		
	STREET		
	CITY	STATE	ZIP
	DATE     /     /	SALES MEMO NO.	

## 2.0 LNWSO SPECIFICATIONS

### I. ELECTRICAL

#### A. Processor

1. Z80A CPU (4MHz)
2. Addressing range of 64k bytes

#### B. Program Memory

1. 12k bytes ROM (Level II Basic)
2. 16k bytes RAM

#### C. Graphics Memory

1. 16k x 6 RAM (4116 Type)
2. 1k bytes RAM (Standard TRS-80 characters and graphics)

#### D. Display

1. Ultra high resolution color graphics
  - a. Pixel densities of 384 x 192 in eight colors utilizing RGB monitor and color mapping
2. High resolution TRS-80 compatible color graphics
  - a. Pixel densities of 128 x 192 in eight colors; RGB output; composite color video (NTSC) output
3. Ultra high resolution B/W graphics
  - a. Pixel densities of 480 x 192, mixed with standard TRS-80 characters and graphics. This mode allows software driver programs which can display 80 characters by 24 lines with standard 5 x 7 matrix.
4. High resolution B/W graphics with eight (8) levels of gray scale. This mode is also compatible with standard TRS-80 graphics and text.
5. Standard TRS-80 character set and graphics (128 x 48)
6. Upper and lower case character sets
7. Reverse video

8. RGB, composite video B/W, composite video color (NTSC), RF output B/W and color

E. Cassette

1. Standard TRS-80 500 baud cassette interface
2. Hi-speed 1000 baud cassette interface

F. Power Supply

1. Powers both the computer and the system expansion board
2. Overvoltage protection
3. Short circuit protection
4. Thermal shutdown
5. Four (4) supplies:
  - a. +12V @ 1.5 A
  - b. -12V @ 20.0 mA
  - c. + 5V @ 4 A
  - d. - 5V @ 1 mA

G. Expansion Bus

1. 40 pin TRS-80 bus compatible with the LNW System Expansion Board and all other TRS-80 compatible peripherals.

## II. SOFTWARE

- A. 100% software compatible with any software generated for the Radio Shack's TRS-80 Model I, Level II computer.



### 3.0 Parts List

The following parts lists are grouped into two major sections. These sections are Parts List by Component Number and Composite Parts List.

#### 3.1 Parts List by Component Number

##### 3.1.1 / INTEGRATED CIRCUITS PARTS LIST

U-	1	74S04	63	74LS244	122	74 S157
	2	280A	64	not used	123	NOT USED
	3	74LS244	65	74LS244	124	74S74
	4	74LS241	66	74LS32	125	74LS373
	5	74LS373	67	74LS175	126	74LS174
	6	74LS138	68	74LS02	127	74LS166
	7	not used	69-72	not used	128	74LS174
	8	74LS175	73	74LS138	129	74LS257
	9	75452	74	74LS30	130	COLOR ROM
10-14	not used		75	ROM A1	131	not used
	15	74LS32	76	ROM B1	132	not used
	16	74LS05	77	ROM C1	133	74123
	17	74LS241	78	ROM A	134-136	not used
	18	74LS244	79	ROM B	137	74LS04
	19	74LS11	80	ROM C	138	74 S174
	20	74C86	81	74LS08	139	74S157
	21	TL084	82	74LS86	140	74LS157
22-27	not used		83	74LS153	141	74LS374
	28	74LS08	84	74LS166	142	74LS157
	29	74LS08	85	74LS10	143	74LS374
	30	74LS05	86	SPARE	144	74LS157
	31	74S74	87	74S161	145	74LS157
	32	74LS241	88	74LS157	146	MC1372
	33	74LS30	89-96	4116(200NS)	147-150	not used
	34	74LS240 *	97	74LS157	151	74LS32
	35	74LS139	98	74LS374	152	74LS32
	36	74LS32	99	74LS373	153	74LS74
	37	74C04	100	MCM6674	154	74LS20
	38	74LS132	101	74LS166	155	74S74
39-45	not used		102	74LS20	156	74LS393
	46	74S74	103	74S175	157	SPARE
	47	74S74	104	74S74	158	SPARE
	48	74LS04	105	74LS157	159	74LS10
	49	not used	106-111	4116(250NS)	160	74S161
	50	74LS04	112	74LS157	161	74S161
	51	74LS00	113	SPARE	162	7405
	52	74LS10	114	2114(450NS)	163-166	not used
	53	74LS244	115	2114(450NS)	167	74LS161
	54	74LS139	116	74LS174	168	74LS08
	55	74LS08	117	74LS174	169	74LS11
56-59	not used		118	74LS04	170	74LS02
	60	74LS00	119	74S04	171	74LS32
	61	74LS02	120	74LS123	172	SPARE
	62	74LS244	121	74S74		

\* DO NOT INSTALL IF RADIO SHACK KEYBOARD IS USED.

### 3.1.2 RESISTORS

(1/4 watt, 5% unless otherwise indicated)

R#					
1	150 ohm	52	4.7K	103	470
2	680	53	10K	104	470
3	4.7K	54	10K	105	1.5K
4	680	55	33	106	5.6K
5	4.7K	56	33	107	<del>5.6K</del> 4.7K
6	4.7K	57	1K	108	360 NOTE 1
7	220	58	33	109	2K
8	220	59	33	110	47 NOTE 1
9	4.7K	60	33	111	470 NOTE 1
10	1K	61	33	112	75 NOTE 1
11	1K	62	150	113	not used
12	10K	63	470	114	not used
13	1K	64	200K	115	1.5K
14	4.7K	65	33	116	3.6K
15	1K	66	33	117	750
16	330	67	470	118	330
17	120	68	4.7K	119	not used
18	1.8K	69	100	120	not used
19	270	70	33	121	not used
20	10K	71	33	122	not used
21	75	72	33	123	1K NOTE 1
22	47	73	33	124	220 NOTE 1
23	100	74	33	125	240 NOTE 2
24	1K	75	1K	126	240 NOTE 2
25	180	76	33	127	240 NOTE 2
26	NOT USED	77	33	128	NOT USED
27	20K	78	1K		
28	3.5K	79	1K		
29	1K	80	56K		
30	4.7K	81	1K		
31	10	82	1K		
32	10K	83	33		
33	1.2K	84	1K		
34	7.5K	85	910		
35	7.5K	86	470		
36	1K	87	270		
37	220K	88	910		
38	20K	89	270		
39	20K	90	910		
40	1.8K	91	390		
41	4.7K	92	1.2K		
42	3K	93	470		
43	10	94	1K POTENTIOMETER		
44	20K	95	470		
45	4.7K	96	1K		
46	10K	97	220		
47	4.7K	98	1K Potentiometer		
48	10K	99	1K Potentiometer		
49	10K	100	470		
50	33	101	470		
51	33	102	470		

## 3.1.2 (cont.)

129 10K Potentiometer NOTE 1  
 130 1K  
 131 100  
 132 1K  
 133 430  
 134 3.3 ohm 1 Watt  
 135 1K  
 136 33  
 137 1K  
 138 1 ohm 1 Watt  
 139 150 1 Watt  
 140 100  
 141 1K  
 142 1K  
 143 4.7K  
 144 50K Potentiometer  
 145 100K Potentiometer

NOTE 1 installed only if graphics option implemented  
 with composite video out of MC1372.

NOTE 2 installed only if RF modulator implemented on  
 output of MC1372.

## 3.1.3 CAPACITORS

(CERAMIC 25V +-20% UNLESS OTHERWISE NOTED, ALL  
 ELECTROLYTICS ARE PC MOUNT UNLESS NOTED)

C #  
 1 47pfd  
 2-6 .1ufd  
 7 .1ufd  
 8 10ufd electrolytic 15vdc, axial mount  
 9 .01ufd  
 10 .01ufd  
 11 .1ufd  
 12 .1ufd  
 13-20 .1ufd  
 21 .001ufd polyester film  
 22 .022ufd mylar 25v  
 23 .047ufd mylar  
 24 .001ufd polyester film  
 25-33 .1ufd  
 34 6.8ufd tantalum electrolytic 15v  
 35-40 .1ufd  
 41 6.8ufd tantalum electrolytic (t.e.) 15v  
 42-46 .1ufd  
 47 6.8ufd t.e. 15v  
 48-55 .1ufd  
 56 6.8ufd t.e. 15v  
 57-59 .1ufd  
 60 6.8ufd t.e. 15v  
 61-64 .1ufd

3.1.3 (contin)  
65 6.8ufd t.e. 15v  
66 .1ufd  
67 33ufd electrolytic axial mount 15v  
68 330pfd  
69 .1ufd  
70 6.8ufd t.e. 15v  
71-75 .1ufd  
76 6.8ufd t.e. 15v  
77-82 .1ufd  
83 150pfd  
84 100pfd mica +-5%  
85-92 .1ufd  
93 not used  
94 50pfd mica +-5% 25v  
95 9-35pfd variable capacitor  
96-101 .1ufd  
102-103 not used  
104 .1ufd  
105 not used  
106 not used  
107 not used  
108-111 .1ufd  
112 56pfd mica +-5% 25v NOTE 2  
113 220pfd  
114 .1ufd  
115 not used  
116 .1ufd  
117 not used  
118 6.8ufd t.e. 15v  
119 4.7ufd electrolytic 15v  
120 10ufd electrolytic 15v  
121 2200ufd 25v electrolytic axial  
122-123 6.8ufd t.e. 15v  
124 .1ufd  
125 22ufd tantalum electrolytic 20v  
126 .1ufd  
127-129 6.8ufd t.e. 15v  
130 .1ufd  
131 100ufd electrolytic 16v  
132-134 6.8ufd t.e. 15v  
135 .1ufd  
136 22ufd electrolytic 15v axial  
137 100ufd electrolytic 25v  
138 150pfd  
139 470pfd  
140 9-35pfd variable capacitor  
141 15000ufd electrolytic 15v  
142 .1ufd NOTE 2

## 3.1.4 MISCELLANEOUS SEMICONDUCTORS

Q #	DESCRIPTION
1	<del>2N3906</del> 2N3904
2	2N3904 2N3906
3	7805(T0220)
4	7812(T0220)
5	not used
6	MPU131
7	7805
8	7805
9	7805
10	7805
11	79L12
12	MPU131
13	2N3906
14	2N3904
15	not used
16	not used
17	not used
18	J175(National) or E175(Siliconix) FET

## SCR#

1	6A 50VRMS SCR (R/S No. 276-1067)
2	6A 50VRMS SCR

## 3.1.5 DIODES

CR#	VALUE
1	1N4001 1A 50PIV NOTE 1
2	1N914 SILICON SIGNAL 75PIV
3	NOT USED
4-10	1N914 — do not use CR 9-10
11	14V ZENER (1N5244 or equivalent)
12,13	1N4001
14	5.1V ZENER (1N5231 or equivalent)
15	BRIDGE 50V 4A (R/S No. 276-1146)
16	1N4001
17	BRIDGE 50V 4A (██████████) MOT. MDA 970-1 *
18	NOT USED
19-23	1N4001
24	6.2V ZENER (1N5235, R/S No. 276-561)

NOTE 1 Installed only if composite video output of MC1372 is desired.

\* HEATSINK THIS PART

## 3.1.6 MISCELLANEOUS

Y1 16.00mhz CRYSTAL  
 Y2 3.5794545 mhz CRYSTAL  
 L1 .08 uHENRY variable inductor NOTE 2, NOTE 3  
 L2 .56 uHENRY  
 RLY1 5VDC relay (R/S No. 275-216)

IC SOCKETS	QUANTITY
14 PIN low Profile	47
16 PIN low Profile	48
18 PIN low Profile	3
20 PIN low Profile	16
24 PIN low Profile	6
40 Pin low Profile	1
8 Pin low Profile	1

NOTE 2 *INSTALL ONLY IF RF MOD. OUTPUT IS INSTALLED*

## NOTE 3

3 turns 22GA solid wire air core wrapped on diameter of a pencil

## 3.2 Composite Parts List

## 3.2.1 INTEGRATED CIRCUIT COMPOSITE LIST

DESCRIPTION	QUANTITY	SYMBOLIC NAME
74LS00	2	U51,60
74LS02	3	U61,68,170
74C04	1	U37
74S04	2	U1,119
74LS04	4	U48,50,118,137
7405	1	U162
74LS05	2	U16,30
74LS08	5	U28,29,55,81,168
74LS10	3	U52,85,159
74LS11	2	U19,169
74LS20	2	U102,154
74LS30	2	U33,74
74LS32	6	U15,36,66,151,152,171
74LS74	1	U153
74S74	7	U31,46,47,104,121,124,155
74C86	1	U20
74LS86	1	U82
74123	1	U133
74LS123	1	U120
74LS132	1	U38
74LS138	2	U6,73
74LS139	2	U35,54
74LS153	1	U83
74LS157	6	U88,97, <del>133</del> , 140 142,144,145
74LS161	1	U167
74S161	3	U87,160,161
74LS166 or 74166	2	U84,101
74LS174	2	U116,117
74LS175	2	U8,67
74S175	1	U103
74LS240	1	U34 *
74LS241	3	U4,17,32
74LS244	6	U3,18,53,62,63,65
74LS373	2	U5,99
74LS374	3	U98,141,143
74LS393	1	U156
75452	1	U9
MC1372	1	U146
MCM6674	1	U100
4116 (200NS)	8	U89-96
2114 (450NS)	2	U114,115
2716(L2 ROMSET)	6	U75-80
TL084 OPAMP	1	U21
Z80A CPU	1	U2
74S174	1	U138
74S157	2	U122, U139

\* DO NOT INSTALL IF RADIO SHACK KEYBOARD IS USED

## 3.2.1 (cont)

## GRAPHICS OPTION

-----  
 INCLUDES 1. HIGH RESOLUTION B/W GRAPHICS  
 2. LOWRES COLOR GRAPHICS

74LS157	2	U105,112
74LS166	1	U127
74LS174	2	U126,128
74LS257 (TI ONLY)	1	U129
74LS373	1	U125
4116 (250NS)	6	U106-111
COLOR ROM	1	U130

(AVAILABLE FROM LNW RESEARCH,  
 PROGRAMMING INST. IS ON PG. 30)



### 3.2.2 RESISTOR COMPOSITE PARTS LIST (1/4 watt, 5% unless otherwise indicated)

DESCRIPTION	QUANTITY	SYMBOLIC NAME
1 ohm 1watt	1	R138
3.3 1watt	1	R134
10	2	R31,43
33	18	R50,51,55,56,58-61,65,66 70-74,76,77,83
47	2	R22,110
75	2	R21,112
100	4	R23,69,131,140
120	1	R17
150	2	R1,62
150 1watt	1	R139
180	1	R25
220	4	R7,8,97,124
240	3	R125-127
270	3	R19,87,89
330	2	R16,118
360	1	R108
390	1	R91
430	1	R133
470	11	R63,67,86,93,95,100-104,111
<del>560</del>	<del>2</del>	<del>R107</del>
680	2	R2,4
750	1	R117
910	3	R85,88,90
1K	22	R10,11,13,15,24,29,36,57,75,78, 79,81,82,84,96,123,130,132,135, 137,141,142
1.2K	2	R33,92
1.5K	2	R105,115
1.8K	2	R18,40
2K	1	R109
3K	1	R42
3.5K	2	R28,116
4.7K	<del>2</del> 13	R3,5,6,9,14,30,41,45,47,52,68,143,107
5.6K	1	R106
7.5K	2	R34,35
10K	8	R12,20,32,46,48,49,53,54
20K	4	R27,38,39,44
56K	1	R80
200K	1	R64
220K	1	R37

### POTENTIOMETERS

1K Mini Pc	3	(R/S Cat No. 271-333)	R94,98,99
10K Mini Pc	1	(R/S Cat No. 271-335)	R129
50k Pc	1	(R/S Cat No. 271-219)	R144
100K Pc	1	(R/S Cat No. 271-220)	R145

## 3.2.3 COMPOSITE CAPACITOR PARTS LIST

(NOTE: all capacitors are PC mount 15v unless otherwise noted)

DESCRIPTION	QUANTITY	SYMBOLIC NAME
47pfd ceramic	1	C1
50pfd mica +- 5%	1	C94
56pfd mica +- 5%	1	C112
9-35pfd variable	2	C95,140
100pfd mica +- 5%	1	C84
150pfd ceramic	2	C83,138
220pfd ceramic	1	C113
330pfd ceramic	1	C68
470pfd ceramic	1	C139
.001ufd poly film	2	C21,24
.01ufd ceramic	2	C9,10
.022ufd mylar	1	C22
.047ufd mylar	1	C23
.1ufd ceramic	90	C2-7,11-20,25-33,35-40, 42-46,48-55,57-59,61-64, 66,69,71-75,77-82,85-92, 96-101,104,108-111, 114,116,124,126,130,135,142
4.7ufd electrolytic	1	C119
6.8ufd tantalum	17	C34,41,47,56,60,65,70, 76,118,122,123,127-129, 132-134
10ufd electrolytic	1	C120
10ufd electro.axial	1	C8
22ufd electro.axial	1	C136
22ufd tantalum 20v	1	C125
33ufd electro.axial	1	C67
100ufd electro.16v	1	C131
100ufd electro.25v	1	C137
2200ufd elec.axial 25v	1	C121
15000ufd electrolytic	1	C141

## 3.2.4 COMPOSITE MISCELLANEOUS SEMICONDUCTOR

DESCRIPTION	QUANTITY	SYMBOLIC NAME
2N3904 transistor	2	Q2,14
2N3906 transistor	2	Q1,13
J175(Nat.) FET	1	Q18
MPU131 unijunction	2	Q6,12
7805 (T0220)	5	Q3,7,8,9,10
7812 (T0220)	1	Q4
79L12 (T092)	1	Q11
6A 50PIV SCR	2	SCR1,2

## 3.2.5 COMPOSITE DIODE LIST

QUANTITY	DESCRIPTION
9	1N4001 1A 50 PIV
<del>5</del> 6	1N914 silicon switching 75v PIV
1	1N5231 5.1v Zener .5 watt or greater
1	1N5234 6.2v Zener .5 watt or greater
1	1N5244 14v Zener .5 watt or greater
2	50v 4A inline bridge diode

## 4.0 ASSEMBLY

Due to the density and complexity of the LNWSO Circuit Board, etch and circuit pad widths are quite small and very delicate. Good soldering and assembly practices must be followed explicitly. Use high quality electronic solder, or preferably multicore, resin core solder. Do not use greater than a 30 watt pencil iron, constantly keeping the tip cleaned and tinned. Avoid using excess heat on the board. If parts must be removed while heating components with the iron, gently tug or rock the lead out of the hole. Since the holes are plated through, the plating will be removed with the component lead if care is not exercised.

All LNWSO boards are thoroughly inspected before shipping. However, it is recommended that you make a visual inspection of the board before installing any components.

### 4.1 GENERAL ASSEMBLY INSTRUCTIONS

The purchaser of the LNWSO is assumed to have a certain degree of ability in assembling electronic equipment. Therefore, a detailed step-by-step Assembly Manual containing topics, such as: How to install a resistor, transistor, or I.C., will not be discussed. What the assembly instructions will include are general and specific construction hints that we felt would be useful in making your LNWSO board as easy and simple to build as possible.

Although sockets for the I.C.'s are not required, we feel it is imperative you use them. The circuit pads are delicate and the removal of I.C.'s can cause serious damage to the board. For this reason, we make the following recommendations:

Use high quality I.C. sockets, inspect them visually for defects before installation and take great care not to bend pins under while inserting the sockets into the board. Before soldering the pins of the socket, make sure that all the pins make it through the holes. All components are to be installed on the component side with the silkscreened legend.

When installing the transistors, SCR's and IC Regulators, make sure that the correct part is being installed the proper way. Also, make sure all diodes, electrolytic and tantalum capacitors have been installed with the proper polarity.

We, at LNW Research, can not possibly recommend parts substitution. Let it suffice to say that if the parts called out for in the parts list are used exclusively, flawless operation will result. We can not guarantee operation if substitute parts are used. We also realize that there are those who for one reason or another will find it necessary to substitute parts. The following paragraph is written for these individuals:

There are some common sense guidelines to follow when you are looking to substitute parts. Make sure you consider all the possible differences the part may possess compared to the part called out originally. For example, do not install a 74LS86 into the location of U20 as the part required is a CMOS 74C86. A TTL part, such as, 74LS86 will not function in this location. Also, for another example, do not use a 74LS161 in place of a 74S161 at U87 as this circuit requires the speed advantage of the 74S161. Be sure to consider power consumption when substituting IC's. If 74TTL was substituted for 74LSTTL at every spot on the board, it would draw more than three times the power from the five volt supply. In the worst extreme, some parts are not pin for pin compatible between 74TTL and 74LSTTL families.

#### 4.2 SPECIFIC ASSEMBLY INSTRUCTIONS

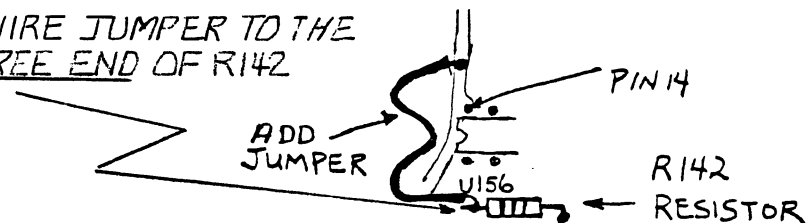
##### SPECIAL WIRING

The following three special assembly instructions should be accurately incorporated:

1. Add a jumper wire (insulated wire) from:  
JP15 to JP16  
(NEAR U47 , NEAR U87 )

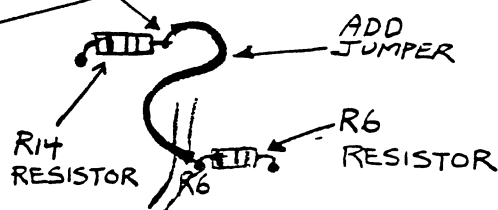
2. Install R142 as shown below:

WIRE JUMPER TO THE  
FREE END OF R142



3. Install R14 as shown below:

WIRE JUMPER TO THE  
FREE END OF R14



##### POWER SUPPLY

The connector locations of J5\* and J2 were designed to use .156 center spacing 6 pin molex type connectors. J5\* connects to the power transformer and J2 connects to the LNW System Expansion Board.

Care must be taken in wiring a transformer to the LNW30 board. You must fuse the incoming AC with a 1 Amp fuse. Otherwise, damage may occur to components on the board or the transformer.

\* USE RIGHT ANGLE TYPE WITH SQUARE PINS CAPABLE OF HANDLING 5 AMPERES.

Connect J5 pin 2 and 3 to the outer terminals of the 18VAC 2A transformer. The center tap is not used. Connect J5 pin 5 and 6 to the center tap and the outside terminal of the 9 VAC 4A transformer, respectively.

#### KEYBOARD

The keyboard is connected to J4 if using an LNW keyboard or J3 when using a Radio Shack keyboard.

The spacing of J4 allows for a .100 inch center, dual row 40 pin header. You may make the keyboard connection with ribbon cable or point to point wiring. Example, J4 pin 1 on the LNW800 board goes to J4 pin 1 of the LNW keyboard.

The connection of the Radio Shack keyboard to J3 on the LNW80 board is done point to point. Make sure pin 1 on the keyboard matches with pin 1 of J3.

#### HIRES B/W VIDEO WIRING

The LNW80 has two separate outputs for connection to a display. The HIRES B/W video output (between cassette Jack and J1) outputs composite B/W video for connection to a standard B/W video monitor (Leedex, BMC, Sanyo, Hitachi, etc.). An RF modulator can also be connected to this output if desired. The spacing for this output allows the mount of a standard 2 pin molex connector. Use 75 ohm shielded cable (RG58 or RG174) in wiring to a monitor or modulator and keep this cable as short as possible (<5 ft.) to prevent loss of picture quality.

#### COLOR NTSC VIDEO/RF

The output of J6\* pin 1 can be wired to deliver a color or black and white display in either NTSC non-interlaced composite video or RF modulated on Channel 3 or 4. The specific details on wiring for each of these different configurations follows:

#### COMPOSITE VIDEO

Install all components as specified in the parts lists with the exception of the following list:

##### DO NOT INSTALL THESE PARTS:

R125  
R126  
R127  
R128  
C112  
L1

The parts unique to composite video output must be installed and are noted specifically as such in the parts list.

*\* 8 conductor .156 header (right angle)*

NOT USED

(Signature)

The output of this connector can be wired with shielded coaxial 75 ohm wire or a right angle two conductor malex pin can be wired to the board at pins 1 and 2 at J6. Pin 1 is the signal and pin 2 is ground.

#### RF MODULATOR

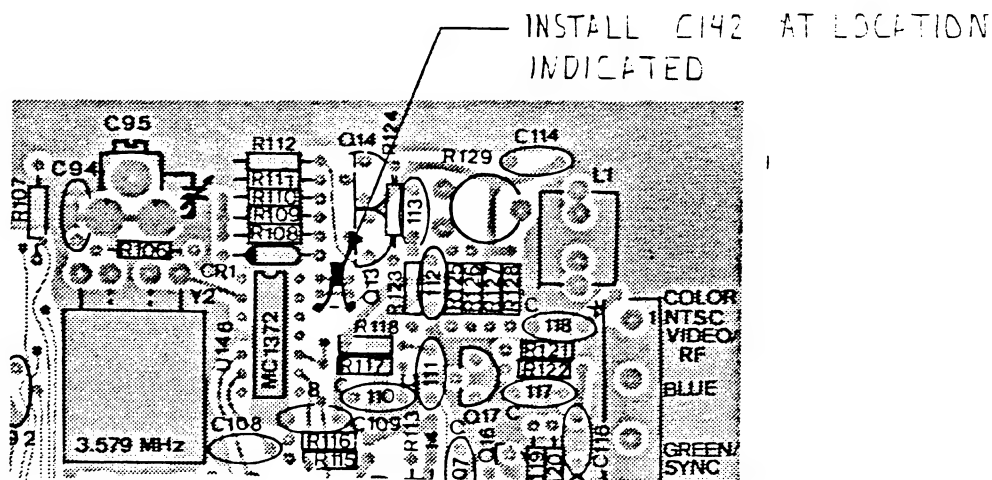
Install all components as specified in the parts list with the exception of the following list:

DO NOT INSTALL THESE PARTS:

R108  
R110  
R112  
R123  
R124  
CR1

The parts unique to the RF modulator must be installed and are noted specifically as such in the parts list. Be sure to keep the lead lengths of these parts as short as possible.

INSTALL C142 AS DESCRIBED BELOW:

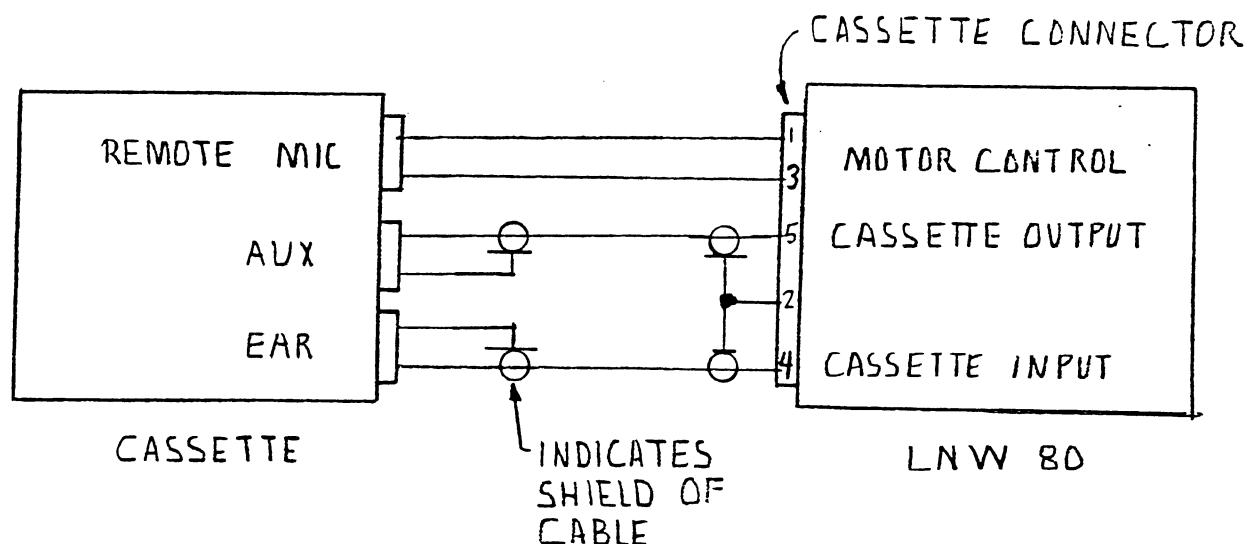


The RF output is taken from pins 1 and 2 of J6 and can be wired to a 75 ohm coaxial cable (RG 58, 174) to a standard 75 to 300 ohm transformer (or antenna switch) for connection to a television set.



## CASSETTE

Connecting the LNW80 to a cassette is shown schematically below:



The type of connectors used for tape decks are typically miniature phone plugs for the earphone and Aux inputs and subminiature phone plugs for the remote Mic input. The connector used for the LNW80 can be either a P.C. mount Din Jack or you may just hard wire the cassette connections to the LNW80 board.

Wire the cassette using shielded cable. Wire shield of cable to outside of connector. You may also purchase a "Cassette to TRS80 Model 1 Cable" available through Radio Shack.

The remote Mic Jack function is to keep the cassette motor off until the computer begins loading or saving a program. If you do not wish to use this function, you may manually turn the recorder/player in record or play mode to start the save or load functions.

## LNW SYSTEM EXPANSION

You need not install the Termination Resistors (R34 to R57), MUX Capacitor (C14), or any of the power supply components on the LNW System Expansion Board when using it with the LNW80 board.

If you have already installed all components onto the expansion board, you need only to cut the power and ground wire to the termination resistors and disconnect the power supply jumpers: JP1-JP2, JP3-JP4, JP7-JP8, JP9-JP10 and JP11-JP12. You must remove C14, however.

If you intend to mount the LNW80 Board and the Expansion Board into the LNW80 case, because of size limitations you will need to remove all power supply components on the Expansion

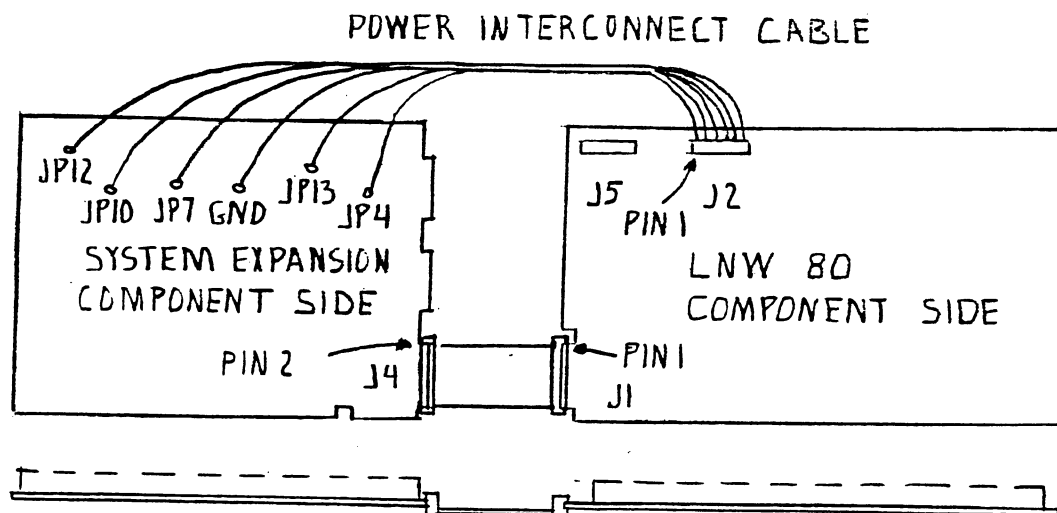
Board. Many of the components on the Expansion power supply are usable on the LNW80 power supply.

You are now ready to install the following interconnect cable as indicated below:

LNW80	LNW EXPANSION	VOLTAGE
J2 pin 1	JP4	+5V
J2 pin 2	JP2	+5V
J2 pin 3	JP12	+12V
J2 pin 4	JP8	-5V
J2 pin 5	JP10	-12V
J2 pin 6	GND	GND

Verify the above voltages on the System Expansion before installing any of the components on the board. If you have installed all the components onto the Expansion Board, verify the voltages at the LNW80 connector J2 before connecting cable and verify wirings.

Figure .. below shows the connection of the LNW80 to the Expansion Board.



### 4.3 INITIAL TEST AND ADJUSTMENTS

The following is step by step Power up Procedure

#### STEP 1: POWER SUPPLY

No IC's should be installed at this time and the power supply jumpers must not be initially installed (JP1 to JP2; JP3 to JP4; etc.).

Turn system power on and measure the following voltages:

REGULATED VOLTAGE	TEST POINT
+ 5V +/- .3V	JP1; JP3; JP5
+ 5V +/- .3V	J2 Pin 1; J2 Pin 2 (If used)
+12V +/- .5V	JP9
-12V +/- .5V	JP7
- 5V +/- .3V	JP11

Turn power off and solder all power supply jumpers indicated below:

JP1 to JP2  
JP3 to JP4  
JP5 to JP6  
JP7 to JP8  
JP9 to JP10  
JP11 to JP12  
JP13 to JP14

Reapply power and measure all supply voltages as you first did.

After all voltages are present, you can install all components that you are to use. Remember, never install or remove components with power on.

#### STEP 2: VIDEO ADJUSTMENTS

Before powering up the first time center the following controls: R94, R98, R99, R144, R145.

The RF modulator on the LNW80 will display all modes of display with exception of MODE 3 (HIRES COLOR). On power up, MODE 0 will be displayed. (At this point what is displayed on the display is relatively unimportant compared to being able to see the display at all).

A. Tune your Television to Channel 3.

B. Apply power to the LNW80 board. What you should see is a strange pattern (possibly out of horizontal or vertical sync) that is being caused by the LNW80. If you fail to see a pattern of this type try tuning your T.V. to channel 2, 4, or 5. If you cannot find anything check the wiring in the area of the RF modulator, the wiring to the T.V. and recheck the power supply.

C. Adjust the video oscillator adjustment C140 till the picture locks in horizontal and vertical sync. If it cannot adjust, make sure all components are correct and installed properly. If the video adjusts but will not lock in, verify that U133, U146, U162, and Y2 are installed as specified.

D. Now do a more accurate adjustment of C140 noting that to either side of the optimum adjustment the picture is intermittently jittery.

E. Now fine tune your T.V. for the clearest and noise free picture. Note that L1 can be adjusted to change the modulation frequency. Spreading the turns farther apart increases the frequency (higher channel number) and squeezing the turns together lowers the modulation frequency.

F. Now adjust R144 for optimum horizontal position and R145 for optimum vertical position.

### STEP 3: POWER-UP SEQUENCE

When applying power to the LNWS0 board, the BREAK (BRK) key should be depressed. An alternative with power already applied, hold the BREAK key along with the RESET (RST) keys. The screen will display:

MEMORY SIZE?

### STEP 4: KEYBOARD

Verify that the CAPS LOCK switch is in the depressed position. If it is not than the characters displayed will not be the standard characters that you are accustomed to seeing. Verify that all characters can be displayed on the monitor, e.g.: 0-9, a-z, ., @, etc.. Verify also that when the SHIFT key is depressed that the upper case characters will be displayed similar to what is on the keys.

↑	Will be displayed as "["
←	Back space one character position
→	Space 8 characters forward
↓	Line feed
{	Will display "\"
}	Will display "^"
[	
]	
CLEAR	Clears display
BREAK	When running a program this key will cause it to terminate

## STEP 5: RAM/ROM TEST

Type in the following simple program. It will test your memory and just by its operation will test the ROM circuits also. The numbers that will be displayed should be the large characters. If this does not occur check the appropriate circuits for problems.

```

1 REM      MEMORY TEST
5 REM THIS IS A SIMPLE TEST OF YOUR MEMORY
6 REM EACH MEMORY LOCATION IS TESTED BY
7 REM USING THE GOSUB INSTRUCTION. IT
8 REM SHOULD RUN CONTINUOUSLY. IF IT STOPS
9 REM THERE IS SOME PROBLEM.
10 CLS:PRINTCHR$(23)
20 PRINT @470, MEM: IF MEM<100 THEN RUN ELSE GOSUB 20

```

## STEP 6: HIGH SPEED/LOW SPEED TESTING

Using the simple RAM/ROM test that you ran before, time the program through one complete cycle (going to zero) at the HIGH SPEED settings (refer to section 8 on the various switch positions). Break the program and switch to LOW SPEED (either forced LOW SPEED or selected LOW SPEED), wait a few seconds and run the program, again timing it. It should now take about twice as long to run. Below is the approximate times for a 16K system to run this program:

HIGH SPEED	35 seconds
LOW SPEED	67 seconds

The reason that it did not run twice as fast is that the CPU is executing mostly out of ROM, which has wait states, and not RAM, which has no wait states.

## STEP 7: CASSETTE TEST

Refer to section 6.0 for cassette operation.

## STEP 8: GRAPHICS TEST AND ADJUSTMENT

Inverse video operation can be tested by entering OUT 254,1. Mode 0 graphics mode can be tested by running the following program.

```

10 REM      MODE 0 TEXT AND GRAPHICS TEST
15 LET Y=0
20 REM
30 FOR X=15360 TO 16383
35 IF Y>192 LET Y=0
40 POKE X,Y
50 LET Y=Y+1
60 NEXT X

```

A3...A0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
A6...A4		D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0	D4 D0
000	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
001	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
010	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
011	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
100	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
101	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
110	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
111	R0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
	R7	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

With the CAPS LOCK switch on all the standard characters and graphics should be displayed. Running the above program with the CAPS LOCK switched off all the characters of the 6674 and the graphics characters will be displayed.

#### STEP 9: TESTING THE HIGH RESOLUTION GRAPHICS MEMORY

THE HIGH RES MODE 1 can be tested by running the HIGH RESOLUTION GRAPHICS TEST on the following page.

#### STEP 10: COLOR GRAPHICS TEST AND ADJUSTMENTS

- 1.Run "COLOR BAR TEST PROGRAM" and wait for it to complete.
- 2.Measure the voltage at pin 6 of U146.Record this value.It should measure between 1.25 and 1.75 volts.
- 3.While measuring the voltage at pin 5 of U146 adjust R99 so that the voltage is the same as the recorded value.
- 4.While measuring the voltage at pin 7 of U146 adjust R98 so that the voltage is the same as the recorded value.
- 5.Adjust R94 so that pin 9 of U146 measures .75 volts DC.
- 6.Adjust the tint and color on your color monitor or television for 7 color bars which from left to right should be white,green,yellow,red,magenta,blue,blue-green.

```
10 REM          HIGH RESOLUTION GRAPHICS TEST
20 REM          CASSETTE (16K) VERSION
30 CLS
40 PRINT "LNW RESEARCH HIGH RESOLUTION GRAPHICS TEST"
45 REM DELAY BEFORE STARTING TEST
50 FOR Z=0 TO 1000
60 NEXT Z
70 OUT 254,2
80 FOR X=32512 TO 32533
90 READ D
100 POKE X,D
110 NEXT X
120 POKE 16526,0:POKE 16527,127
125 LET Y=1
130 FOR Z=0 TO 4
140 REM      NOW POKE DATA TO BE OUTPUT TO USR ROUTINE
150 POKE 32522,Y
155 GOSUB 170
160 LET Y=Y*2
161 NEXT Z
162 LET Y=0
166 POKE 32522,0
167 GOSUB 170
168 PRINT "ALL MEMORY LOCATIONS TESTED"
169 END
170 FOR X=0 TO 16383
180 A=USR(X)
190 LET A=A AND 63
200 IF A=Y THEN GOTO 230
205 PRINT "MEMORY LOCATION FAILED TO READ OR WRITE CORRECTLY"
207 PRINT "ADDRESS      EXPECTED DATA      ACTUAL DATA"
210 PRINT X;Y;A
220 STOP
230 NEXT X
240 RETURN
270 DATA 205,127,10,219,254,246,8,211,254,54,0,0,110,38,0
280 DATA 230,247,211,254,195,154,10
```

```
10 REM          COLOR BAR TEST PROGRAM
20 REM          CASSETTE (16K) VERSION
30 REM THIS TEST SHOULD GENERATE THE FOLLOWING COLORS:
35 REM WHITE GREEN YELLOW RED MAGENTA BLUE BLUE-GREEN BLACK
36 CLS:PRINTCHR$(23)
40 PRINT "LNW RESEARCH COLOR BAR TEST "
45 REM DELAY BEFORE STARTING TEST
50 FOR Z=0 TO 1000
60 NEXT Z
70 OUT 254,4
72 FOR X=15360 TO 16383
74 POKE X,255
76 NEXT X
80 FOR X=32512 TO 32533
90 READ D
100 POKE X,D
110 NEXT X
120 POKE 16526,0:POKE 16527,127
125 FOR X=0 TO 12288
130 FOR Y=0 TO 7
135 FOR Z=0 TO 7
150 POKE 32522,Y*9
180 A=USR(X)
190 LET X=X+1
200 NEXT Z
210 NEXT Y
220 LET X=X-1
230 NEXT X
240 END
270 DATA 205,127,10,219,254,246,8,211,254,54,0,0,110,38,0
280 DATA 230,247,211,254,195,154,10
```



```

00100      ;THIS IS THE USR CALL TO WRITE
00110      ;AND THEN READ BACK FROM GRAPHICS RAM
00120      ;THE ADDRESS IS PASSED INTO HL PAIR
00130      ;BY THE USR CALL AND ROUTINE AT A7F
7F00      00140      ORG      7F00H
7F00 CD7F0A 00150      CALL   INPADR ;GET THE ADDRESS OF THE GR. RAM
7F03 DBFE   00160      IN      A,(0FEH);INPUT FROM PORT 254
7F05 F608   00170      OR      8      ;SET GRAPHICS RAM ENABLE BIT
7F07 D3FE   00180      OUT     (0FEH),A;OUTPUT TO PORT 254
7F09 3600   00190      LD      (HL),0 ;OUTPUT POKED DATA
7F0B 00     00200      NOP                    ;DELAY FOR WRITE TO FINISH
7F0C 6E     00210      LD      L,(HL) ;INPUT FROM GRAPHICS RAM
7F0D 2600   00220      LD      H,0      ;CLEAR H REG
7F0F E6F7   00230      AND     0F7H    ;TURN OFF GRAPHICS RAM ENABLE BIT
7F11 D3FE   00240      OUT     (0FEH),A;OUTPUT TO PORT 254
7F13 C39A0A 00250      JP      BASIC  ;BACK TO BASIC RETURN WITH HL
0A7F      00260      INPADR EQU     0A7FH ;ROUTINE THAT PUTS VARIABLE IN HL
0A9A      00270      BASIC  EQU     0A9AH ;ROUTINE THAT PUTS HL INTO VAR.
0000      00280      END
00000 TOTAL ERRORS

```

```
BASIC 0A9A 00270 00250
INPADR 0A7F 00240 00150
```

## 5.0 SYSTEM CONFIGURATION

### ROM CONFIGURATION

The LNWSO will accept three versions of ROMS, these being the two and three ROM sets from Radio Shack's Level II TRS-80 or the six ROM set from LNW Research. The following configuration on P1 must be properly selected for the LNWSO system to operate. The following configurations are required for the various types of ROM:

1. LNWSO's 6 ROM, install ROM A1 at U75, ROM B1 at U76, ROM C1 at U77, ROM A at U78, ROM B at U79, ROM C at U80.

Connect: P1-2 to P1-15  
P1-4 to P1-13  
P1-5 to P1-12  
P1-7 to P1-10

2. Radio Shack's 3 ROM set, install ROM A at U78, ROM B at U79, ROM C at U80.

Connect: P1-1 to P1-16  
P1-3 to P1-14  
P1-5 to P1-12  
P1-7 to P1-10

3. Radio Shack's 2 ROM set, install ROM A/B (8044364) at U78, ROM C (8044732) at U80.

1. DO NOT install R50, R51

2. wire jumpers

from	to
U19-10	U55-1
U19-11	U55-2
U55-3	U64-10(P1-10)

3. connect:

M to O

O to L

**P1-4 to P1-13**

## NTSC COLOR ROM LISTING

NTSC Color ROM U130 is a 32 X 8 open collector ROM part #82S23. The following is the listing for U130 the NTSC color ROM (Pre-programmed U130 ROM is available from LNW Research):

ADDRESS	DATA (HEX)
0	6C
1	D5
2	CC
3	7A
4	FD
5	EA
6	75
7	6B
8	6F
9	6F
10	6F
11	6F
12	6F
13	6F
14	6F
15	6F
16	AE
17	AE
18	AE
19	AE
20	AE
21	AE
22	AE
23	AE
24	6F
25	6F
26	6F
27	6F
28	6F
29	6F
30	6F
31	6F

FIGURE .. LNW80 NTSC COLOR ROM

## 6.0 SYSTEM OPERATION

It is recommended that you use the following reference manuals:

Level II Basic Reference Manual  
TRS-80 Micro Computer Technical Reference Handbook

Both of which are available through Radio Shack.

### LNW80 POWER-UP SEQUENCE

When applying power to the LNW80 board, the BREAK (BRK) key should be depressed. An alternative with power already applied, hold the BREAK key along with the RESET (RST) keys. The screen will display:

MEMORY SIZE?

### LNW80 POWER-UP SEQUENCE WITH EXPANSION BOARD

First apply power to the disk drive and insert a TRS-80 compatible DOS diskette. Close the disk door and apply power to both the System Expansion and the LNW80. The screen will display:

DOS READY

### CASSETTE OPERATING INSTRUCTIONS

Due to the design of the cassette circuit different volume level settings will be compensated for to provide a very easy to use and reliable cassette interface. In addition, data rates of either 500 baud or 1000 baud can be used.

Normal Radio Shack tapes can be loaded with the LNW80 in the LOW SPEED mode. The cassette transfer rate is 500 baud in this mode.

You may save programs from the computer to the cassette at either the 500 baud rate (Radio Shack compatible speed) or at 1000 baud (LNW80 speed). When saving programs at 1000 baud, switch the LNW80 to HIGH SPEED and save the program as described below.

Saving tapes at 1000 baud gives you the advantage of saving and loading programs in less than half the time compared to the Radio Shack's compatible speed. Care must be taken, however, to keep track of what speed tape you are using. For example, if a program is saved at 500 baud, it can not be loaded at 1000 baud.

When trying to rewind a tape, you must unplug the MIC remote plug, as this line is only turned on during a CLOAD or a CSAVE operation.

## SAVING A PROGRAM ON CASSETTE

Place recorder/player in RECORD mode (be sure the proper connection is made and the cassette tape has been rewound to the proper position). Verify proper LNWSO speed. Enter CSAVE "FILE NAME". This will turn on the cassette and save the program on tape. When the program is loaded, the computer will respond with READY.

The FILE NAME that you use can be any alphanumeric character except double quotes (").

## LOADING A PROGRAM FROM CASSETTE

Place recorder/player in the PLAY mode (be sure connection is made and cassette tape is rewound to the proper position). Verify proper LNWSO speed. Due to the design of the cassette circuit the volume setting is not critical. However, set the volume to about midrange. Enter CLOAD "FILE NAME". This will turn the cassette on and begins loading.

Note that the computer will begin loading only when it encounters the first letter of the file name that you entered in. For example, if you enter CLOAD "TEST", the computer will search through the tape until it encounters a file beginning with "T" and will ignore all others. If you enter CLOAD and do not specify a file name the first program encountered will be loaded. If you enter CLOAD and do not specify a file name, the first program encountered will be loaded.

When the program begins loading an asterick will appear on the upper right hand corner of the display. A short time later, a second asterick will appear but it will be flashing. This will indicate that the program is being loaded properly. If the second asterick does not appear after a short time or appears and does not flash, reset the volume level and try loading again. There may be a slight difference in volume settings between 500 baud and 1000 baud tapes. Verify also that you have the proper speed setting. After the loading is complete, the computer will respond with READY.

When recording over prerecorded tapes, problems may be encountered when loading these tapes. The reason is that the original program may not be completely erased. A solution to this problem is to place a shorting plug in the auxiliary input and place the player in RECORD mode. This will completely erase the tape with the minimum amount of noise. Or you may also use a commercially available tape eraser.

## VERIFYING A TAPE

After loading a tape into the computer, verification can be made by using the command CLOAD? "FILE NAME". To use this, rewind the tape to the start of the program that is to be

compared with the program in the computer. Enter CLOAD? "FILE NAME" and this will begin the cassette. If there is an error, the message "BAD" will appear. In this case, reload the program cassette.

## 7.0 LNW80 GRAPHICS: AN INTRODUCTION

The LNW80 supports four different graphics modes. These graphics modes are selected by I/O port 254 (hex FE). The definition of port 254 is as follows:

D0- Inverse Video (Mode 0,1 Only)  
 D1-  
 D2- Mode Control  
 D3- Graphics RAM Enable  
 D4-D7- Reserved (Do Not Use)

MODE CONTROL		MODE
D2	D1	
0	0	"0" LORES 128 x 48 mixed with text
0	1	"1" HIRES 480 x 192 mixed with LORES
1	0	"2" LORES Color 128 x 192 in 8 colors
1	1	"3" HIRES Color on-off control of 384 x 192 pixels with 128 x 16 (8 colors) color mappings. This mode exceeds NTSC video BANDWIDTH and must be used with RGB monitor.

### MODE DESCRIPTION

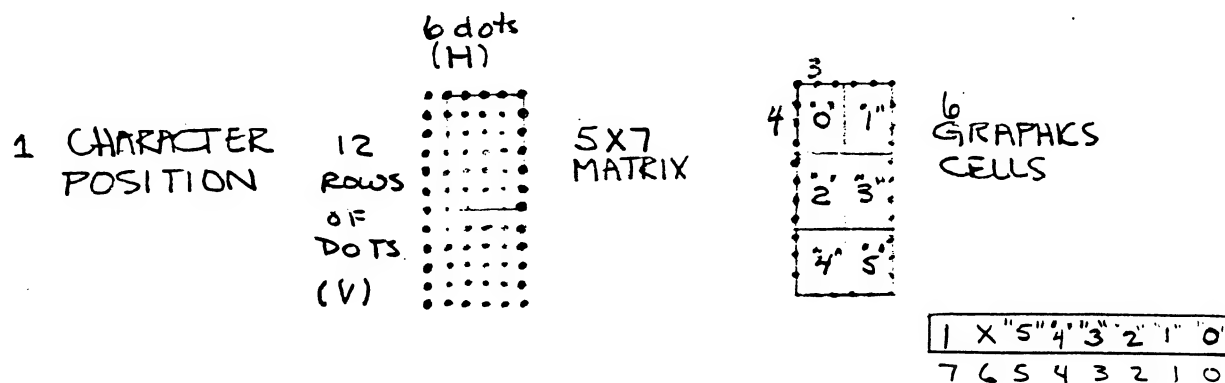
#### LORES MODE "0"

This is the text and graphics mode standard in the other '80 computers'. The graphics memory is located at 3C00 to 3FFF (Hex). Mode 0 addressing is as specified below.

#### MODE 0 ADDRESSING

0	0	1	1	1	1	LINE				CHARACTER			
15	14	13	12	11	10	9	8	7	6	5	4	3	2 1 0 (Address)

The least significant 6 bits specify the character position (A0-5) and A6-9 specifies the line. The graphics and text character position consists of six horizontal dots by twelve vertical rows. The diagram for this character position is shown below.

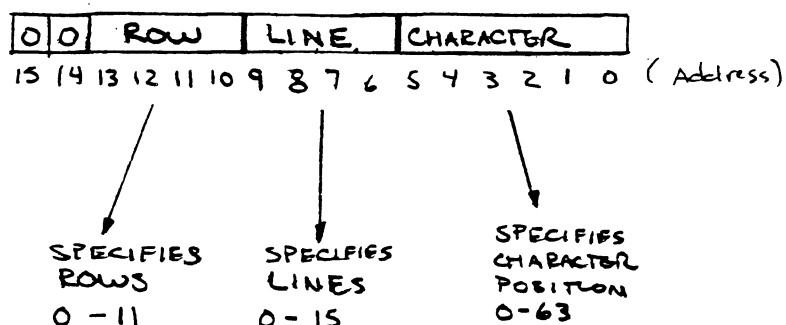


LORES text characters are displayed as a 5 x 7 matrix utilizing the character generator MCM6674. The 5 x 7 format allows one dot space between characters and 5 dot spaces between lines. The mode 0 graphics character comprises 3 horizontal dots by 4 vertical dots. In one character position, there are six graphics cells. With data bit seven on bits 0-5 select all possible combinations of graphics characters. Note that data bit 6 is not used. Due to the large amount of literature published on this graphics mode, no further discussion is presented. For more details refer to "Level II Basic Reference Manual" and "TRS-80 Graphics (RS #62-208)."

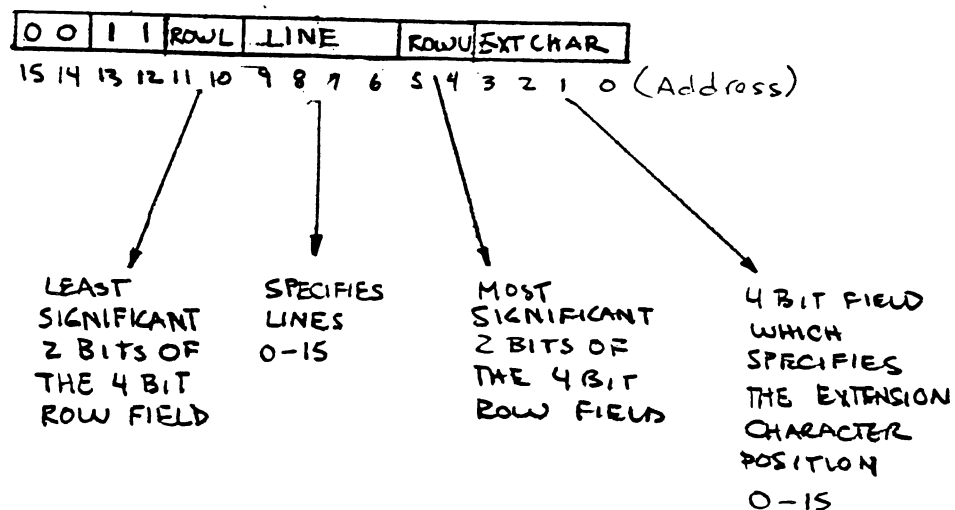


## HIRES MODE 1

This is the high resolution (480 x 192) graphics mode mixed with low resolution (mode 0) text and graphics. The 16k x 6 graphics memory allows individual control of 480 x 192 dots. Each location in the graphics memory holds 6 bits or 6 sequential horizontal pixels. The addressing of this graphics memory is not simple X-Y addressing but is optimized for rapid graphic character generation. The video memory map is broken into two regions. The 384 x 192 inner region addressing is specified by the following figure:

384 x 192 INNER REGION

The extension region 96 x 192 adds additional 16 character position the standard 64 for a total of 80. Refer to the following chart for details on addressing this region:

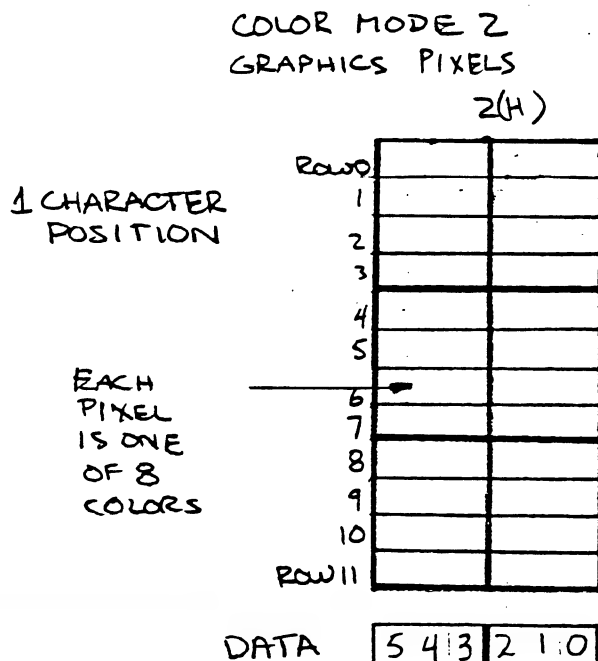
96 x 192 EXTENSION REGION

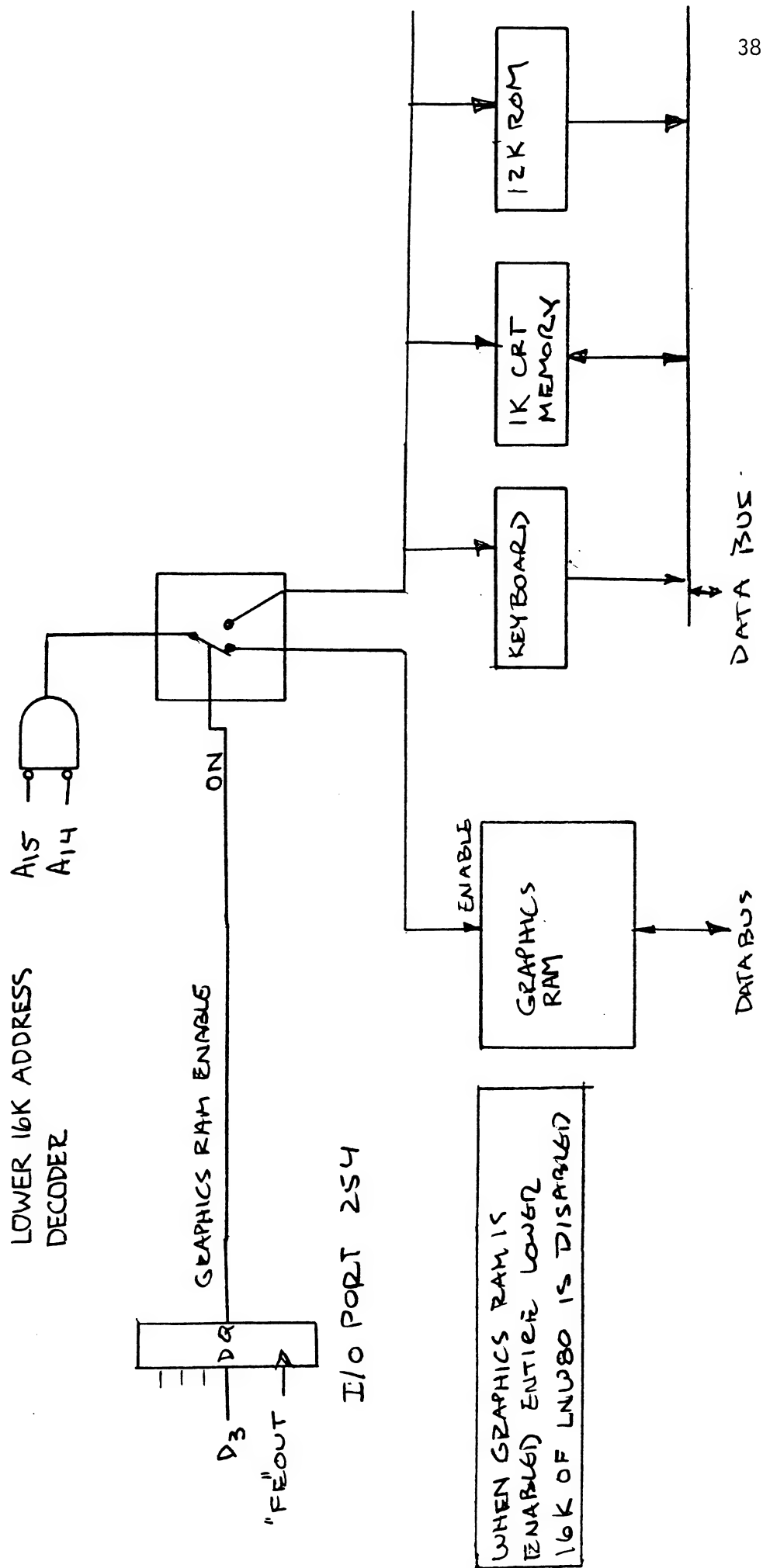
## ACCESSING THE GRAPHICS RAM

The graphics RAM is located at the lower 16k of LNWS0 address space. Note that this is also where the ROM's, keyboard, mode 0 CRT memory and miscellaneous I/O is mapped. I/O port 254 bit-D3 selects which devices are enabled. With D3=1, the graphics memory is enabled at the lower 16k. With D3=0, the keyboard, CRT RAM, 12k ROM and anything else which might be mapped in the lower 16k of the LNWS0 address space, are all enabled such that when they are addressed they will respond. The following drawing illustrates this bank switching operation. NOTE that since the Level II ROM's are also disabled by D3=1, using the OUT command in basic to turn this bit on will be fatal to the computer since the computer will execute out of graphics RAM instead of ROM.

## LORES COLOR - MODE 2

This color mode is the highest resolution mode possible for NTSC composite video. The following figure shows the relationship between the color mapping and the mode 0 graphics pixel for one character position. Outlined in dark borders is the mode 0 graphics pixel.





Four color pixels comprise one mode 0 graphics pixel, since the mode 0 pixel must be "on" for the color pixel to be displayed; here are two ways of using this color mode:

1. Color Compatible - Existing B/W graphics games can be easily converted to color if the objects on the screen usually stay within certain regions of the screen. By mapping color regions in the graphics memory prior to running the game or program, when the game turns on a graphics cell, the color mapped in the graphics memory will be displayed. If the figure displayed is not a graphics character (i.e. a text letter) the dot rate of the luminance will exceed the bandwidth of NTSC color video and hence either the character will be blurry or the color will be wrong. The small character mode of text is especially difficult to reproduce in color while the large characters (32 characters/line) will display very nicely in full color.

2. 128 x 192 color graphics - New programs can be written to take advantage of the resolution and number of colors by simply turning on all the mode 0 graphics cells and selecting one of eight colors (including black) for the color pixel.

The addressing of the color pixels is similar to the high resolution B/W mode (mode 1) with the character position row and line specifying a given address. Each address holds two adjacent color pixels each of which contain three bits of information to specify the color. The fixed background color is represented by all ones (7), which is black.

GRAPHIC  
MEMORY  
ADDRESSING

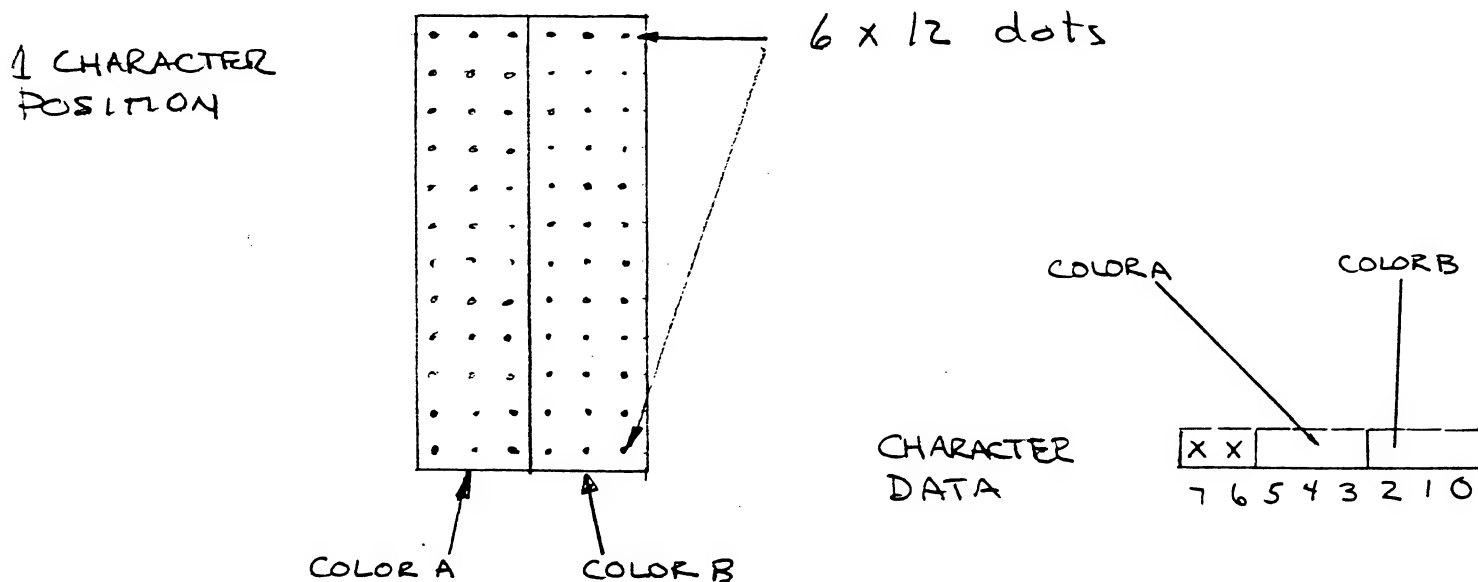
00	ROW	LINE	CHARACTER
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			

OR	5	4	3
	2	1	0
	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0
	1	0	1
	1	1	0
	1	1	1
	COLOR		
	WHITE		
	GREEN		
	YELLOW		
	RED		
	MAGENTA		
	BLUE		
	BLUE-GREEN		
	BLACK		

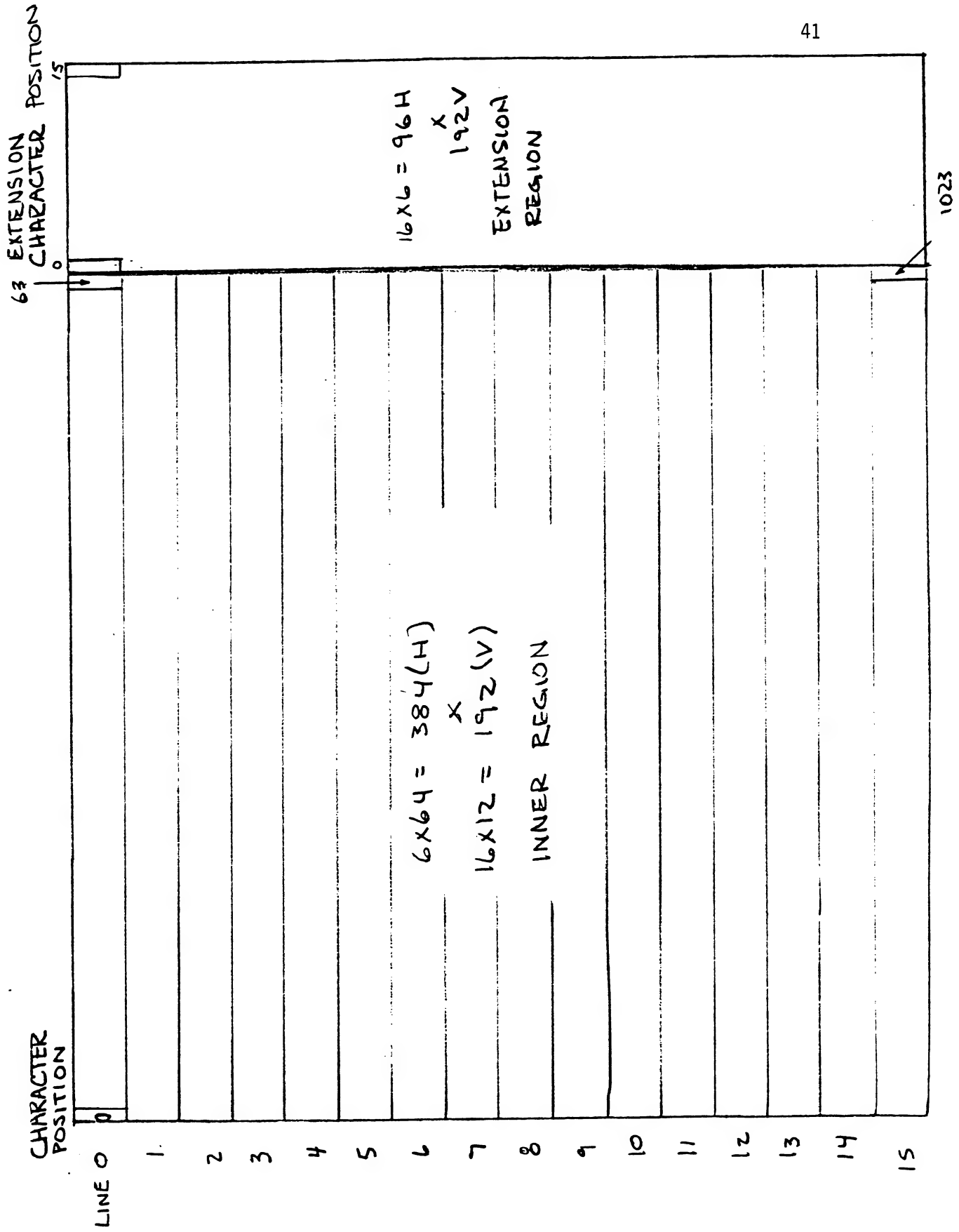
### MODE 3 - HIGH RESOLUTION COLOR GRAPHICS

This color mode provides on-off control of  $384 \times 192$  dots (with the same addressing as inner region addressing for Mode 1 high resolution B/W). The color is defined by the mode 0 memory. It is noted that the extension region ( $96 \times 192$ ) should be cleared since color information will be invalid in this region.

NOTE: IC's U131 and 132 are not listed in the parts list for the LNWS0 because they are used only for RGB (Mode 3) operation. U130 (color ROM) must be replaced with "RGB" and various resistor values around U130 must be changed according to the specific interface requirements of the various RGB monitors. Further details on RGB configuration will be provided along with the purchase of the RGB ROM.



# VIDEO MEMORY MAP



Most graphics applications require the ability to set, reset, and test any individual pixel given the X and Y coordinates. Since the X and Y coordinates do not hold an easy relationship to the address of the graphics RAM, a fast method of translation is needed. Although, equations can be derived to calculate the point based on the addressing charts given, a simpler (and faster) method can be employed using a basic program to poke a machine language user routine into RAM and then poke a translation table into RAM. Once this table is generated, it can be used by the USR routine to evaluate the graphics RAM address relatively fast. Since USR calls can pass a 16 bit variable to the USR routine, the X value (which is greater than 8 bits) is passed in this manner. The Y coordinate can be passed in 8 bits so it is poked to the location in the USR call so it can be used quickly. Machine language routines, can also use this translation program by generating the table in the machine language routine. This program should pose no difficulty to even novice assembly language programmers. If necessary, the table could even be appended to the machine language program itself. The following basic program includes all the necessary routines to set, reset, and point from the high resolution graphics memory. This program is listed for both disk and non-disk applications. In this example program, all initialization is done up to line 220. Your own program can simply generate the X and Y coordinates and using lines 250 and 260 as an example call the USR FLN to set, reset, and text the point. The assembly language source code for the data statement follows the basic program listings.

#### GRAPHICS CHARACTER GENERATION

Besides using the capabilities of the Mode 1 (HIRES) display for graphics, this mode can be used to extend the CRT text handling capabilities of the LNW80. Character generation programs can be written which allow variable character sets (i.e. Foreign language, programmable, etc.) with as many as 80 characters on a line and up to 24 lines of display. Since the

addressing of the HIRES graphics memory (Mode 1) is optimized for this, programs written for this can be implemented easily. Even modifications to editing programs can be done to add descenders, subscripts, superscripts, etc.

#### AN EXAMPLE:

Assume a word processing outputs a character to the screen by supplying character position (0-79), the line number (0-15) and the actual character (ASCII). The new display driver program flow chart could be drawn as below:

```

0 REM THIS POKES 2 TABLES,THE FIRST ONE GENERATES 2 BYTES FOR
1 REM EACH HORIZONTAL COORDINATE(X). THIS TWO BYTE PAIR
2 REM CONSISTS OF (1)THE CHARACTER POSITION(0-79) AND (2) THE
3 REM ONE OF SIX PATERN SELECTING THE PIXEL WITHIN THE
4 REM CHARACTER POSITION. THE SECOND TABLE IS THE VERTICAL.IT
5 REM CONSISTS OF 192 LOCATIONS EACH OF WHICH HOLDS THE
6 REM ROW(D4-7) AND THE LINE(D0-3).THE TABLES START AT 30000.
10 LET X=30000
20 FOR Y=0 TO 79
30 GOSUB 100
40 NEXT Y
50 LET X=31024
55 FOR L=0 TO 15
60 FOR R=0 TO 11
65 LET N=(16*R)+L
70 POKE X,N
75 LET X=X+1
80 NEXT R
85 NEXT L
90 GOTO 171
100 LET N=1
101 FOR Z=0 TO 5
120 POKE X,Y
130 LET X=X+1
140 POKE X,N
150 LET X=X+1
155 LET N=N*2
160 NEXT Z
165 RETURN
166 REM THIS ROUTINE POKES THE MACHINE LANGUAGE USR PROGRAM
168 REM INTO RAM STARTING AT LOCATION 79FOH(31216) TO 7A90
169 REM (31376).
171 FOR X=31216 TO 31376
172 READ Y
173 POKE X,Y
174 NEXT X
175 REM THIS POKE COMMAND GIVES THE ENTRY POINT OF THE
177 REM ONE USR CALL. THE LOW ORDER BYTE MUST BE CHANGED
179 REM TO POINT TO ONE OF THE OTHER ROUTINES IF DESIRED.
181 REM 200 POKE 16526,LOW BYTE:POKE 16527,HIGH ORDER
182 REM REMEMBER THAT THESE ADDRESS LOCATIONS ARE DECIMAL
185 REM TO SELECT SET,RESET,POINT USE THE FOLLOWING VALUES:
187 REM SET POKE 16526,240:POKE 16527,121
189 REM RESET POKE 16526,243:POKE 16527,121
191 REM POINT POKE 16526,246:POKE 16527,121
193 REM ONCE YOU HAVE POKED THESE VALUES OUT,YOU NEED ONLY
195 REM POKE THE LOW ORDER BYTE TO CHANGE TO A DIFFERENT
197 REM ROUTINE (IE. POKE 16526,246).
199 REM
200 POKE 16526,240:POKE 16527,121
202 REM 210 CLS CLEARS LOWRES SCREEN
204 REM 220 OUT 254,2 TURNS HIRES (MODE 1) ON
205 REM 230 FOR X=0 TO 479 BUMPS THROUGH ALL X POSITIONS
206 REM 240 FOR Y=0 TO 191 BUMPS THROUGH ALL Y POSITIONS
207 REM 250 POKE 31257,Y POKES Y VALUE TO 31257 (IN USR)
208 REM 260 A=USR(X) X IS PASSED TO USR ROUTINE

```

CASSETTE VERSION



```
210 CLS
220 OUT 254,2
230 FOR X=0 TO 479
240 FOR Y=0 TO 191
250 POKE 31257,Y
260 A=USR(X)
270 NEXT Y
280 NEXT X
290 END
300 DATA 195,67,122,195,88,122,195,113,122,205,127,10
310 DATA 1,48,117,41,9,126,254,64,242,35,122,205,19,122
320 DATA 203,60,203,29,203,60,203,29,201,35,70,33,48,121
330 DATA 17,0,0,25,102,111,203,37,203,37,201,205,19,122
340 DATA 203,37,203,37,203,4,203,4,203,60,203,29,203,60
350 DATA 203,29,203,60,203,29,203,60,203,29,124,198,48
360 DATA 103,201,205,249,121,219,254,246,8,211,254,126
370 DATA 176,119,219,254,230,247,211,254,195,154,10,205
380 DATA 249,121,219,254,246,8,211,254,120,238,255,71
390 DATA 126,160,119,219,254,230,247,211,254,195,154,10
400 DATA 205,249,121,219,254,246,8,211,254,126,160,194,133
410 DATA 122,33,0,0,195,136,122,33,1,0,219,254,230,247
420 DATA 211,254,195,154,10
```

```

0 REM  THIS POKES 2 TABLES,THE FIRST ONE GENERATES 2 BYTES FOR
1 REM  EACH HORIZONTAL COORDINATE(X). THIS TWO BYTE PAIR
2 REM  CONSISTS OF (1)THE CHARACTER POSITION(0-79) AND (2) THE
3 REM  ONE OF SIX PATERN SELECTING THE PIXEL WITHIN THE
4 REM  CHARACTER POSITION. THE SECOND TABLE IS THE VERTICAL.IT
5 REM  CONSISTS OF 192 LOCATIONS EACH OF WHICH HOLDS THE
6 REM  ROW(D4-7) AND THE LINE(D0-3).THE TABLES START AT 30000.
10 LET X=30000
20 FOR Y=0 TO 79
30 GOSUB 100
40 NEXT Y
50 LET X=31024
55 FOR L=0 TO 15
60 FOR R=0 TO 11
65 LET N=(16*R)+L
70 POKE X,N
75 LET X=X+1
80 NEXT R
85 NEXT L
90 GOTO 171
100 LET N=1
101 FOR Z=0 TO 5
120 POKE X,Y
130 LET X=X+1
140 POKE X,N
150 LET X=X+1
155 LET N=N*2
160 NEXT Z
165 RETURN
166 REM  THIS ROUTINE POKES THE MACHINE LANGUAGE USR PROGRAM
168 REM  INTO RAM STARTING AT LOCATION 79F0H(31216) TO 7A90
169 REM  (31376).
171 FOR X=31216 TO 31376
172 READ Y
173 POKE X,Y
174 NEXT X
175 REM  THESE NEXT THREE STATEMENTS ASSIGN THE 3 USR CALL TO
177 REM  THE INDIVIDUAL ENTRY POINTS.
180 DEFUSR0=&H79F0
190 DEFUSR1=&H79F3
200 DEFUSR2=&H79F6
202 REM      210 CLS          CLEARS LOWRES SCREEN
203 REM      215 CMD"T"      TURNS OFF INTERRUPTS
204 REM      220 OUT 254,2    TURNS HIRES (MODE 1) ON
205 REM      230 FOR X=0 TO 479  BUMPS THROUGH ALL X POSITIONS
206 REM      240 FOR Y=0 TO 191  BUMPS THROUGH ALL Y POSITIONS
207 REM      250 POKE 31257,Y    POKES Y VALUE TO 31257 (IN USR)
208 REM      260 A=USR0(X)     X IS PASSED TO USR ROUTINE
210 CLS
215 CMD"T"
220 OUT 254,2
230 FOR X=0 TO 479
240 FOR Y=0 TO 191
250 POKE 31257,Y
260 A=USR0(X)

```

DISK VERSION

```
270 NEXT Y
280 NEXT X
290 END
300 DATA 195,67,122,195,88,122,195,113,122,205,127,10
310 DATA 1,48,117,41,9,126,254,64,242,35,122,205,19,122
320 DATA 203,60,203,29,203,60,203,29,201,35,70,33,48,121
330 DATA 17,0,0,25,102,111,203,37,203,37,201,205,19,122
340 DATA 203,37,203,37,203,4,203,4,203,60,203,29,203,60
350 DATA 203,29,203,60,203,29,203,60,203,29,124,198,48
360 DATA 103,201,205,249,121,219,254,246,8,211,254,126
370 DATA 176,119,219,254,230,247,211,254,195,154,10,205
380 DATA 249,121,219,254,246,8,211,254,120,238,255,71
390 DATA 126,160,119,219,254,230,247,211,254,195,154,10
400 DATA 205,249,121,219,254,246,8,211,254,126,160,194,133
410 DATA 122,33,0,0,195,136,122,33,1,0,219,254,230,247
420 DATA 211,254,195,154,10
```

79F0	00100	ORG	79F0H	
79F0 C3437A	00101 SET	JP	SETR	;SET ROUTINE ENTRY
79F3 C3587A	00102 RESET	JP	RESR	;RESET ENTRY
79F6 C3717A	00103 POINT	JP	POIR	;POINT ROUTINE
79F9 CD7F0A	00110 ADCAL	CALL	INPX	;GET X POSITION IN HL PAIR
79FC 013075	00120	LD	BC,7530H	;START OF HORIZONTAL TBL
79FF 29	00125	ADD	HL,HL	;DOUBLE HL IN TABLE
7A00 09	00130	ADD	HL,BC	;POINT TO CHARACTER POS. IN TBL
7A01 7E	00140	LD	A,(HL)	;INPUT CHARACTER POSITION
7A02 FE40	00150	CP	64	;IS > THAN CHAR 64 (IN EXTENSION)
7A04 F2237A	00160	JP	P,EXTEND	;YES USE EXT. ALGORITHM
7A07 CD137A	00170	CALL	VERT	;GET ROW.LINE,CHARACTER ADJUSTED
7A0A CB3C	00180	SRL	H	;SHIFT LSB OF H INTO CARRY
7A0C CB1D	00190	RR	L	;GET LSB OF H INTO MSB OF L REG
7A0E CB3C	00200	SRL	H	;SHFT LSB OF H INTO MSB OF L
7A10 CB1D	00210	RR	L	;ONCE AGAIN
7A12 C9	00220	RET		;NOW HL HAS ADDRESS OF GRAPHICS
7A13 23	00240 VERT	INC	HL	;THIS PUTS ROW.LINE INTO H AND
	00245			;PUTS CHARACTER POSITION SHIFTED
	00247			;LEFT TWO BITS INTO L WITH THE
	00249			;TWO LSB SET TO ZERO
7A14 46	00250	LD	B,(HL)	;NOW B REG HAS ONE OF SIX PATERN
7A15 213079	00260	LD	HL,7930H	;START OF VERTICAL LOOKUP TABLE
7A18 110000	00265	LD	DE,0H	;POKE DATA HERE
7A1B 19	00270	ADD	HL,DE	;POINT TO VALUE IN TABLE
7A1C 66	00280	LD	H,(HL)	;PUT ROW.LINE INTO H
7A1D 6F	00290	LD	L,A	;COPY CHARACTER POSITION TO L
7A1E CB25	00300	SLA	L	;SHIFT LEFT ONE PLACE
7A20 CB25	00310	SLA	L	;NOW L HAS LEFT JUSTIFIED CHAR
7A22 C9	00320	RET		
7A23 CD137A	00330 EXTEND	CALL	VERT	;GET VERT. IN H,CHAR IN L,DAT IN B
7A26 CB25	00340	SLA	L	;ROTATE 2 MSB OF ROW AND
7A28 CB25	00350	SLA	L	;PUT THEM IN THE 2 LSB OF H
7A2A CB04	00360	RLC	H	
7A2C CB04	00370	RLC	H	
7A2E CB3C	00375	SRL	H	;NOW SHIFT HL RIGHT 4 PLACES
7A30 CB1D	00380	RR	L	
7A32 CB3C	00390	SRL	H	
7A34 CB1D	00400	RR	L	
7A36 CB3C	00410	SRL	H	
7A38 CB1D	00420	RR	L	
7A3A CB3C	00430	SRL	H	
7A3C CB1D	00440	RR	L	;HL OK NOW
7A3E 7C	00445	LD	A,H	
7A3F C630	00447	ADD	A,30H	;MAKE ADDRESS ABOVE ROW 11
7A41 67	00449	LD	H,A	
7A42 C9	00460	RET		

```

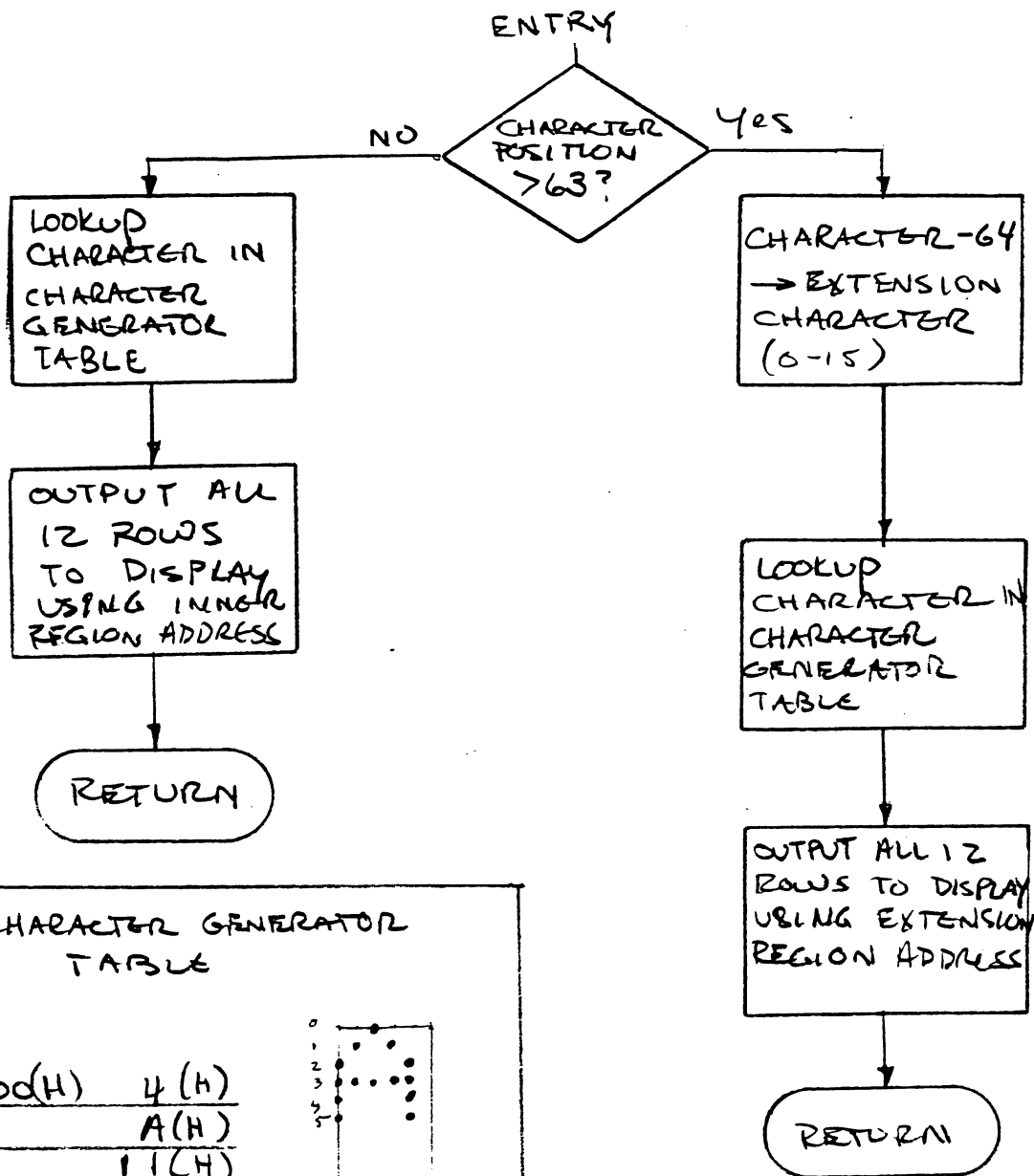
7A43 CDF979    00470 SETR    CALL    ADCAL
7A46 DBFE      00480        IN      A,(0FEH);INPUT FROM 254
7A48 F608      00490        OR      8          ;TURN ON GRAPHICS RAM ENABLE BIT
7A4A D3FE      00500        OUT     (0FEH),A;OUTPUT TO 254
7A4C 7E        00510        LD      A,(HL) ;LD DATA IN A REG.
7A4D B0        00520        OR      B          ;SET BIT
7A4E 77        00530        LD      (HL),A ;WRITE DATA BACK OUT
7A4F DBFE      00540        IN      A,(0FEH);INPUT AGAIN
7A51 E6F7      00550        AND     0F7H      ;TURN OFF GRAPHICS RAM
7A53 D3FE      00560        OUT     (0FEH),A;OUTPUT PORT 254
7A55 C39A0A    00570        JP      RETURN
7A58 CDF979    00580 RESR    CALL    ADCAL
7A5B DBFE      00590        IN      A,(0FEH)      ;INPUT PORT 254
7A5D F608      00600        OR      8          ;SET GRAPHICS RAM ENABLE BIT
7A5F D3FE      00610        OUT     (0FEH),A;OUTPUT TO PORT 254
7A61 78        00620        LD      A,B

7A62 EEFF      00630        XOR     0FFH      ;COMPLEMENT A
7A64 47        00640        LD      B,A
7A65 7E        00650        LD      A,(HL)
7A66 A0        00660        AND     B
7A67 77        00670        LD      (HL),A ;WRITE DATA BACK OUT
7A68 DBFE      00680        IN      A,(0FEH);INPUT AGAIN
7A6A E6F7      00690        AND     0F7H      ;TURN OFF GRAPHICS RAM
7A6C D3FE      00700        OUT     (0FEH),A
7A6E C39A0A    00710        JP      RETURN
7A71 CDF979    00720 POIR    CALL    ADCAL
7A74 DBFE      00730        IN      A,(0FEH)
7A76 F608      00740        OR      8
7A78 D3FE      00750        OUT     (0FEH),A
7A7A 7E        00760        LD      A,(HL) ;GET SIX BITS OF DATA
7A7B A0        00770        AND     B          ;MASK ALL BUT SELECTED BIT
7A7C C2857A    00780        JP      NZ,SETHL ;MAKE L=1 IF NOT ZERO
7A7F 210000    00790        LD      HL,0H      ;MAKE HL PAIR 0
7A82 C3887A    00800        JP      QUIT      ;EXIT
7A85 210100    00810 SETHL  LD      HL,1H      ;SET HL=0001H
7A88 DBFE      00812 QUIT    IN      A,(0FEH)      ;INPUT PORT
7A8A E6F7      00814        AND     0F7H      ;TURN OFF GRAPHICS RAM BIT
7A8C D3FE      00816        OUT     (0FEH),A;OUTPUT TO PORT 254
7A8E C39A0A    00820        JP      RETURN
0A9A          00830 RETURN  EQU     0A9AH
0A7F          00840 INPX    EQU     0A7FH ;THIS PUTS VARIABLE INTO HL PAIR
0000          00850        END
00000 TOTAL ERRORS

```

80 CHARACTER/LINE  
(16 LINES)

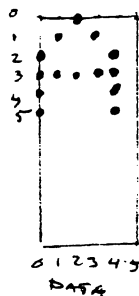
# SIMPLIFIED FLOWCHART



## SAMPLE CHARACTER GENERATOR LOOKUP TABLE

LETTER: A

Row 0	: 3000(H)	4(H)
Row 1		A(H)
Row 2		11(H)
Row 3		1F(H)
Row 4		11(H)
Row 5		11(H)
Row 6		0(H)
Row 7		0(H)
Row 8		0(H)
Row 9		0(H)
Row 10		0(H)
Row 11	: 300B(H)	0(H)



If you choose to have 24 lines of display, only 7 rows of display per line can be allocated with one blank row between lines. In this case, the starting row for each line must be looked up in a simple table and all 8 rows output from data.

## 8.0 CIRCUIT DESCRIPTION

### SYSTEM CLOCK

The LNWSO System Clock is a 16 MHz oscillator, utilizing Y1 and U1 74S04 to form a series resonant circuit. The LNWSO CPU utilizes two (2) microprocessor clock speeds of 4 MHz ("Hi-Speed") and 1.77 MHz ("Lo-Speed"). The 1.77 MHz clock is the compatible clock rate for the TRS-80 Model 1 computer. This clock rate of 1.77 MHz may be used on the LNWSO computer when there is software timing that must be adhered to; i.e. TRS DOS disk timing and the standard TRS-80 500 baud cassette. Synchronous clock switching is incorporated in the speed selection. IC U87, a synchronous 4-bit counter, is used to perform the divide by four (4) for the 4 MHz operation and divide by nine (9) for the 1.77 MHz operation.

#### 1.77 MHZ CPU SPEED (SW1=1)

As SW1 is selecting position 1, U120 pin 1, (clock A input) is constantly being retriggered with 60 Hz (VERTIP Signal) to form the Lo-Speed selection at U120 pin 4, when active low (logic "0") a preset of 1,0,0, will be presented at U87 pins 3,4,5 respectively. This preset will program U87 to divide by nine (9) resulting in a 1.77 MHz CPU clock.

#### 4.00 MHZ CPU SPEED (SW1=OPEN)

This switch position forces the CPU clock to be at 4 MHz. When in this mode, any program written for the standard TRS-80 speed of 1.77 MHz will be executed over 2X faster. However, if there are software timing loops, these loops will also be 2X faster; thus, this mode of operation may not be compatible with some TRS-80 standard software.

SW1 switch selection of center off position will prevent U120 pin 1 (clock A input) from triggering, resulting in a "1" at U120 pin 4 causing a preset of 0,1,1 at U87 pins 3,4,5 respectively. This preset, 0,1,1, will result in the divide by four (4) of the system clock, generating a 4 MHz clock to the CPU.

#### AUTO HI-LO CPU SPEED (SW1=3)

This mode of operation allows the use of any standard TRS-80 disk operation. When the LNWSO accesses the floppy disk, the CPU clock will automatically switch from 4.00 MHz to 1.77 MHz. Thus, total compatibility to the standard disk operation is maintained.

When the disk operation is completed the CPU clock is automatically restored to the "hi-speed" of 4 MHz.

This final SW1 selection of position 3 is an "automatic slow down and up" mode. When the address decode of 37EC (Floppy



Disk Device Address) and IMREQ (Memory Request) is true then U120-4 will be triggered to generate an active Lo. A divide by nine (9) at U87 will create a 1.77 MHz clock to the CPU during the floppy disk read or write access. When U120's one-shot expires, then the CPU clock is automatically and synchronously switched back to the "Hi-Speed" of 4 MHz.

#### FORCELO\* LNWS0 KEYBOARD SPEED SWITCH (LINE LOC.)

FORCELO\*, U29 pin 5, forms a override term in the U120 speed selection. FORCELO\* term is from the LNWS0 keyboard (see LNWS0 Keyboard Section) which will force the U87 to divide by nine (9) resulting in a CPU clock of 1.77 MHz. When the FORCELO term is removed (logic "1") then the CPU speed is determined by SW1 settings. For example, to use standard 500 baud Radio Shack cassette programs, you must depress this key.

#### POWER-UP AND SYSTEM RESET

U32 is a hysteresis input buffer, when C136 charges up to a logic "1" voltage level then the reset is removed from Z80A CPU and the SYSRES\* line. When the Z80A is reset, the next instruction execution will start at location 0000. The system reset switch, SW2, will discharge C120 resulting in a logic zero input to U38 pin 4. When SW2 is depressed an active lo SYSRES\* is generated. The reset function will generate a non-maskable interrupt at U2 (Z80A CPU) pin 17 causing the next CPU instruction execution to be at location 0066H.

#### WAIT, INT\* and TEST\*

The WAIT input to the Z80A CPU will cause the Z80A to extend its cycle, resulting in slowing down the CPU. The LNWS0 utilizes one WAIT function when a ROM read is in progress and 1 or 2 waits when accessing the video memory. These waits are required in the hi-speed mode of 4 MHz to ensure data validity when accessing the slower memory devices. There are no wait states when accessing the program memory (RAM) on the LNWS0 and the LNWS System Expansion's program memory (requiring 200ns or faster RAM's). The wait term is generated by U31 pin 5 the clock to U31 is delayed by U16, since low power Schottky IC are used in address decoding, this clock delay results in proper data setup time to U31. U61 pin 3 is WAITHLD which will increase the wait from the usual one wait state for the Level II ROM's, to two wait states when reading from the video memory. Pin 33 of J1 is the bus WAIT signal, this input may be utilized by other external devices that may wish to pose a wait condition on the Z80A Processor.

The INT\* signal is a maskable interrupt to the Z80A Processor pin 16. The Level II Basic ROM utilizes interrupt mode 1. When the CPU is interrupted, a restart to location 0038H is executed.

Pin 23 of J1 is TEST\* which is a busrequest signal to the Z80A CPU. The CPU responds by tri-stating its data, address and output control signal. Since the Z80A CPU is fully buffered, all the buffers (U3, U4, U17, U18) will also be tri-stated. Once these buffers are tri-stated, any device on the expansion bus may control the function of the LNWSO board. One important consideration is the dynamic program RAM's are refreshed by the Z80A Processor, so whatever controlling device on the expansion bus must consider memory refresh.

RAS\*, MUX, CAS\*

The LNWSO utilizes the 16k x 1 dynamic memories (4116 type) with maximum access time of 200ns. The addressing sequence of events is RAS\* (Row Address Select), MUX (Multiplex), then CAS\* (Column Address Selection) to multiplex the 14 bits of address into two 7-bit parts for the 4116 type dynamic RAM. Figure 1 shows the timing diagram for the memory control signals on a write operation.

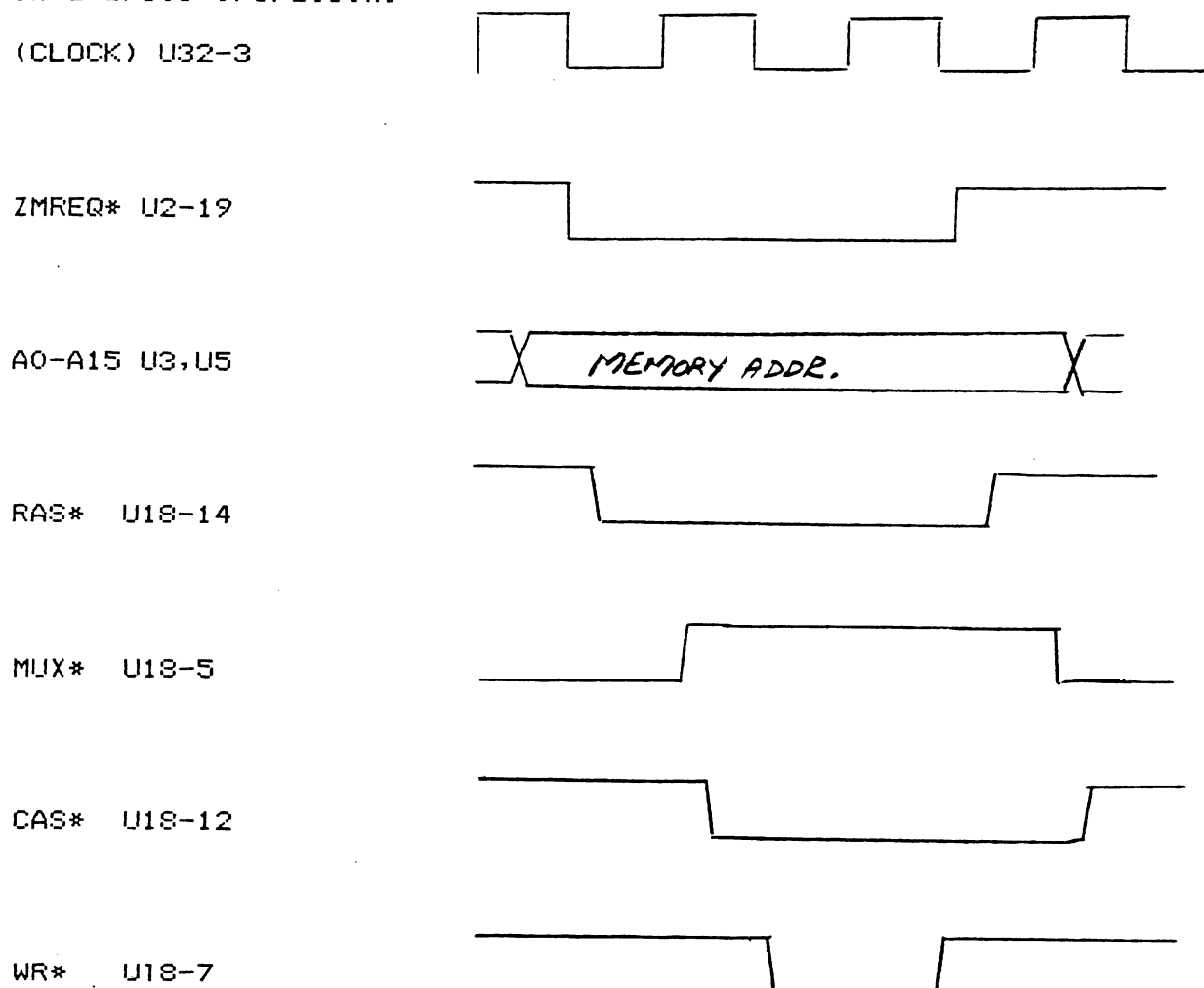


FIGURE 1  
Memory Write Timings

## LNW80 EXPANSION BUS

This 40 pin bus, J1, is equivalent to the TRS-80's 40 pin expansion bus. The exception is the drive capability on the LNW80 is dramatically increased from that of a TRS80.

The following are the signals and their descriptions for J1:

J1	P/N	Signal Name	Description
1		RAS*	Row Address Strobe
2		SYSRES*	System Reset, Low on Power up and Depressing Reset
3		CAS*	Column Address Strobe
4		A10	Address Output
5		A12	Address Output
6		A13	Address Output
7		A15	Address Output
8		GND	Signal Ground
9		A11	Address Output
10		A14	Address Output
11		A8	Address Output
12		OUT*	I/O or Peripheral Write Strobe Output
13		WR*	Write Output Strobe
14		INTACK*	Interrupt Acknowledge
15		RD*	Memory Read Strobe
16		MUX	Multiple RAM Address
17		A9	Address Output
18		D4	Data Bus
19		IN*	I/O or Peripheral Read Input Strobe
20		D7	Data Bus
21		INT*	Maskable Interrupt Input
22		D1	Data Bus
23		TEST*	Bus Request Line Tri-State all Address, Data and Control Line
24		D6	Data Bus
25		A0	Address Output
26		D3	Data Bus
27		A1	Address Output
28		D5	Data Bus
29		GND	Signal GND
30		D0	Data Bus
31		A4	Address Output
32		D2	Data Bus
33		WAIT*	Z80A CPU Wait
34		A3	Address Output
34		A3	Address Output
35		A5	Address Output
36		A7	Address Output
37		GND	Signal GND
38		A6	Address Output
39		N/C	Not Used
40		A2	Address Output

## ADDRESS DECODER

There are several major sections of the LNW80 which are memory mapped. These sections are listed below along with their decoded address. U6 and U35 generate the decodes for the ROM, keyboard, display RAMS, and program RAMS.

ADDRESS		
DECIMAL	HEX	DEVICE
0	<u>0000</u>	
12288	<u>3000</u>	Basic ROM
		Unused
14302	37DE	Communication Status Address
14303	37DF	Communication Data Address
14304	37E0	Interrupt Batch Address
14305	37E1	Disk Drive Select Latch
14308	37E4	Cassette Select Latch
14312	37E8	Parallel Printer Address
14316	37EC	Floppy Disk Controller Address
14336	<u>3800</u>	
14591	<u>38FF</u>	Keyboard
15360	3C04	Display RAM's
16383	<u>3FFF</u>	
16384	4000	16k RAM
32767	<u>7FFF</u>	
65535	FFFF	32k RAM (on the Expansion Board)

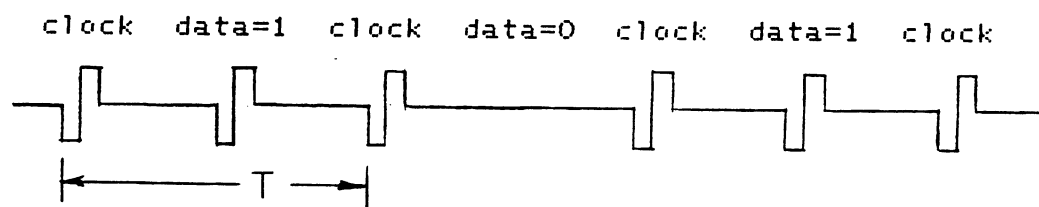
## RAM REFRESH

The LNWS0 utilizes the Z80A/CPU to generate the refresh to the RAM's. The memory refresh address is output on the lower 7 address bits during refresh time. An instruction fetch will increment the refresh register (R).

The LNWS0 uses a "RAS\*" only, where RAS\* will be an active "0" and CAS\* will be at a logic "1" state (off state) during refresh. At refresh time the MUX signal will be a logic "0" state selecting the A0-A7 as the RAM address.

## CASSETTE

Programs are loaded onto tape in serial fashion. The serial data contains both clock and data information as shown below:

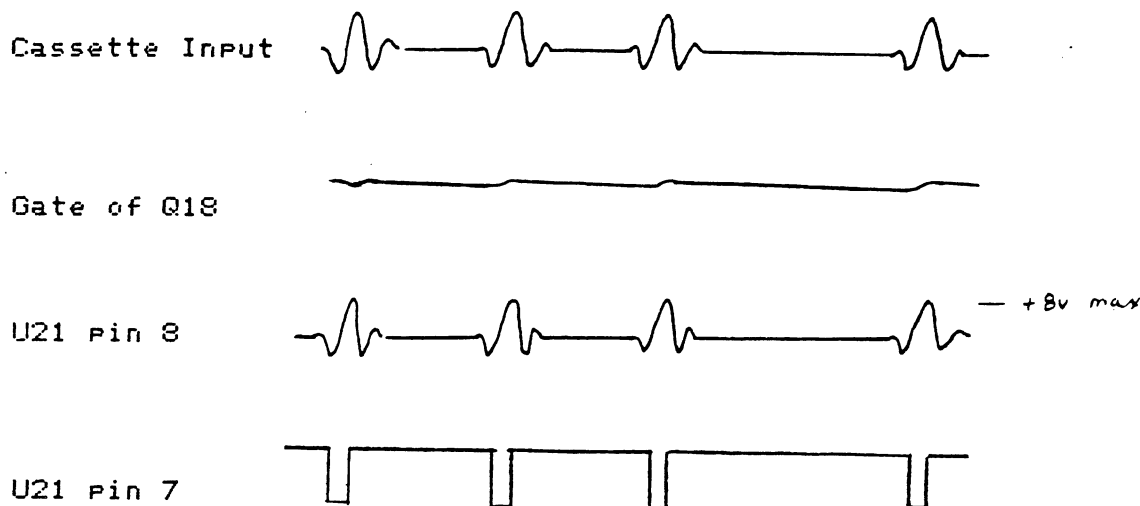


The time "T" is dependent upon whether the computer is in High Speed or Low Speed. In Low Speed the time "T" is 2 ms. In High Speed this time is 1 ms. This timing results in a transfer rate of 500 baud and 1000 baud, respectively.

The cassette routines are resident in the Level 2 ROM's and cassette is accessed as an I/O port. When a CSAVE is entered, the address FF is placed on the Address bus along with the OUT\* signal going low. When this happens D2 will go high which is clocked into U8 pin 12 which turns U9 on and relay K1 on. This shorting of pins 1 and 3 of the cassette connector through K1 will result in turning the cassette motor on. D0 and D1 also get clocked into U8 with timing that results in the above diagram.

The cassette loading operation is accomplished through U21 A, B, and C. Refer to the figure below:

#### Cassette Waveforms



The signal from the cassette is voltage divided by R24 and R25. U21A is a two pole active high pass filter which will eliminate noise. U21B along with U18 function as an automatic gain controlled (AGC) amplifier. The amplitude at U21B pin 8 is peak detected by CR2 and C119 to set an average signal level. The voltage at the gate of Q18 will then be higher as the signal amplitude goes higher. The higher the voltage at the gate, the higher the resistance between the source and drain which will have the effect of lowering the gain of this stage. The lower the gate voltage, the lower the drain to source resistance and the higher the gain. The voltage level of U21B will be controlled to a maximum of about 8.0 volts. U21C is a comparator who's trip level is dependent upon the voltage at U21C pin 5. The output at pin 7 is normally high which will go low when a data or clock signal is encountered.

U38 is a flip flop who is set and reset by U21C pin 7 and FFOUT\*, respectively. The decoded signal FFIN\* will then place the cassette information onto D7.

#### KEYBOARD

The LNWSO keyboard is designed specifically for the LNWSO computer board providing a 63 keypad, an 11 keypad, and all the special functions that are available to you through the LNWSO computer.

A Radio Shack keyboard is also usable on the LNWSO board. However, the special function keys must be hard wired per the

LNW80 keyboard schematic if you use a keyboard other than the LNW80 keyboard.

Do not attempt to use an ascii encoded keyboard, however, as the LNW80 was not designed to be compatible with it.

The keyboard is a scanning type keyboard based on an eight by eight matrix. Normally, all lines are floating until the KYBD\* signal goes low which turns Q1 on and pulls all signals high which indicates a keyboard scan operation.

## SPECIAL KEYBOARD FUNCTIONS

- RETURN: Functions the same as the ENTER key typically on the Radio Shack Computer.
- RESET (RST): Both RST keys must be depressed to reset the computer.
- LINE LOC: Forced LOW Speed switch. When depressed system is in the LOW Speed mode. When not depressed system will run at its normal High Speed.
- CONTROL: This is a special software controlled key. For example, it is used in the ELECTRIC PENCIL Word Processing Program.
- CAPS LOCK: Places the computer in the upper case mode. For example, as in the ELECTRIC PENCIL Word Processing Program.

## POWER SUPPLY

The LNW80 Power Supply section is designed to power both the LNW80 Computer Board and the LNW Expansion Board.

Two Radio Shack or equivalent transformers must be used to provide the necessary AC power. The schematic shows the required voltages that must appear at the transformer (JS) connector.

The Radio Shack part numbers for the transformers are:

18VCT	4A	RS#273-1514
18VCT	2A	RS#273-1515

## +5V SUPPLY

The unregulated AC voltage of the transformer is

rectified by CR17 and filtered by the 15,000 ufd capacitor. This capacitor must be located somewhere off the LNW80 board.

Q3, Q9, and Q10 provide the +5 volt regulated supply for the LNW80 Computer Board. Q7 and Q8 provide the regulated +5 volts for the System Expansion Board.

All +5V outputs are connected through diodes to a summing point at the anode of Q12. If any of these voltages exceeds approximately 6.2V then CR24 will begin to conduct. While the gate of Q12 remains unchanged, the anode voltage will begin to rise higher than the gate. This will cause Q12 to begin conducting which will fire SCR-1 causing F1 to open. This overvoltage protection prevents damage to component due to high voltage.

#### +12V SUPPLY

CR15 rectifies the AC signal which is then filtered by C121. Q4 regulates the voltage to +12 volts. If the voltage at JP9 exceeds 13 volts, CR11 will begin to conduct. While the gate of Q6 remains unchanged, the anode will begin to rise above the gate voltage. This will cause Q6 to begin conducting and result in turning SCR2 on. F2 will then open. The +12 volts are used for both the LNW80 and the Expansion Board.

#### -12V SUPPLY

R138 limits the current, C137 provides DC blocking and CR19 and CR16 provide a voltage doubler. Q11 will then provide a -12 volt regulated output which supplies both the LNW80 board and the Expansion board.

#### -5V SUPPLY

The voltage at the negative lead of C131 is regulated by R133 and CR14 and it is then filtered by C130. This -5 volts is used for both the LNW80 board and the Expansion board.



## 9.0 SCHEMATICS

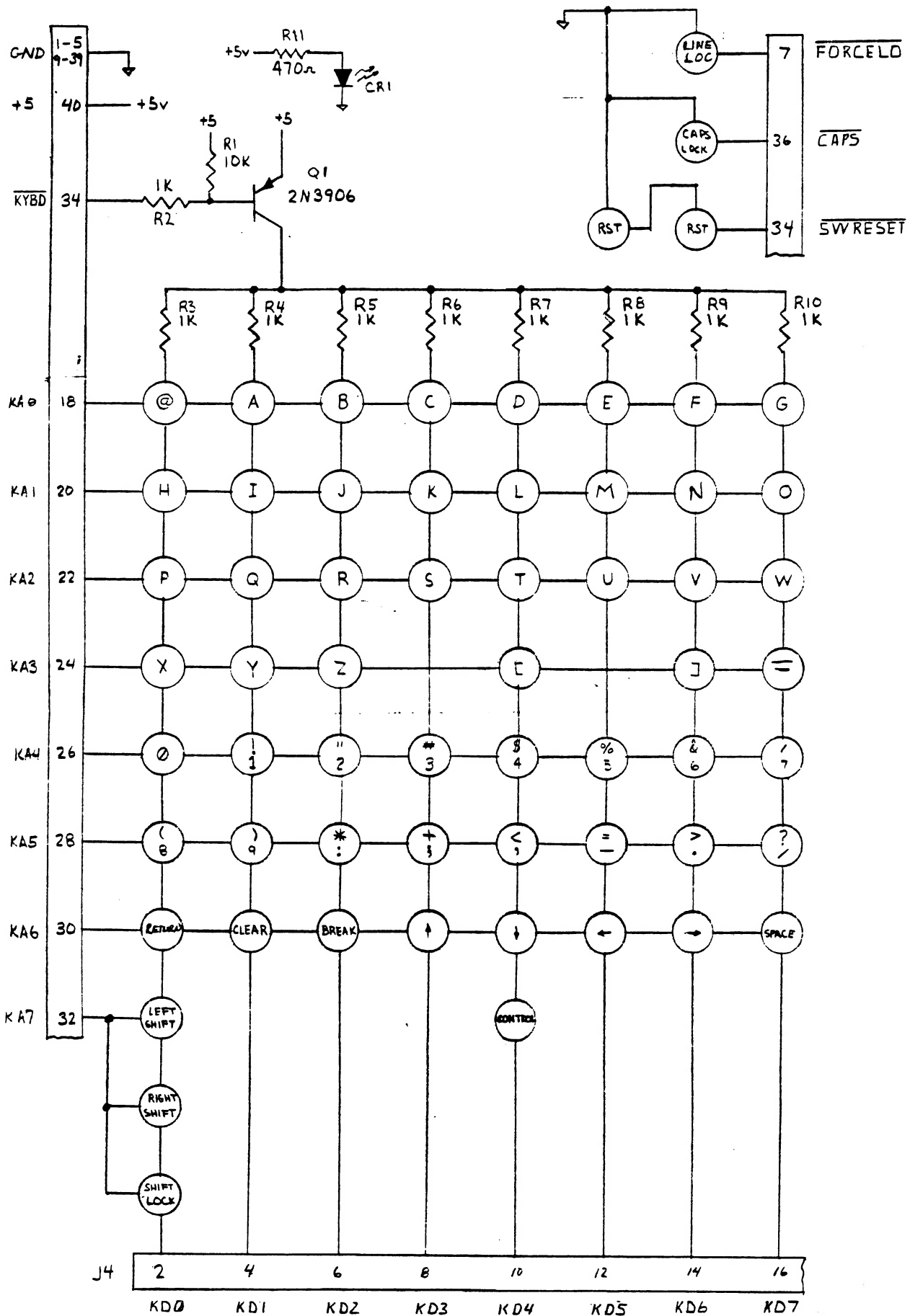
The schematic diagrams show the internal structure of the device. The first diagram shows the overall layout of the device, including the input and output ports, the power supply, and the internal components. The second diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors.

The third diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The fourth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors. The fifth diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The sixth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors.

The seventh diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The eighth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors. The ninth diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The tenth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors.

The eleventh diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The twelfth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors. The thirteenth diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The fourteenth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors.

The fifteenth diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The sixteenth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors. The seventeenth diagram shows the internal structure of the device, including the input and output ports, the power supply, and the internal components. The eighteenth diagram shows a more detailed view of the internal components, including the transistors, capacitors, and resistors.



TO LNWR80 J4

## 10.0 LIMITED WARRANTY

LNW Research warrants the P.C. Board from manufactured defects for a period of ninety (90) days.

LNW Research does not offer or imply any other warranty.

\*TRS-80 is a product of Tandy Corporation.

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# LNW RESEARCH COMPONENT PRICE LISTS

\*KIT80-1\* START UP PART SET . . . . . \$82.00

QUANTITY	DESCRIPTION	DESIGNATION
1	74C04	U37
2	74S04	U1,119
7	74S74	U31,46,47,104,121,124
		155
1	74C86	U20
3	74S161	U87,160,161
1	74S175	U103
1	74LS240	U34
3	74LS241	U4,17,32
6	74LS244	U3,18,53,62,63,65
3	74LS373	U5,99,125
3	74LS374	U98,141,143
1	74LS393	U156
2	2114	U114,115
1	TL084	U21
1	E175	Q18
2	MPU131	Q6,12

\*KIT80-2\* VIDEO PART SET . . . . . \$31.00

QUANTITY	DESCRIPTION	DESIGNATION
1	MC1372	U146
1	NTSC COLOR ROM	U130
1	MCM6674	U100
1	16MHz CRYSTAL	Y1
1	3.57945 MHz CRYSTAL	Y2
1	.56 uH INDUCTOR	L2

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